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DATA SHEET

COMPOUND FIELD EFFECT POWER TRANSISTOR μ PA1556

N-CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

DESCRIPTION

The μ PA1556A is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
 $I_{D(pulse)} = \pm 20$ A
 $R_{DS(on)} = 0.20 \Omega$ TYP. ($V_{GS} = 10$ V)
 $R_{DS(on)} = 0.25 \Omega$ TYP. ($V_{GS} = 4$ V)
- Low Capacitance $C_{iss} = 700$ pF TYP.
- Gate Protector built in.
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

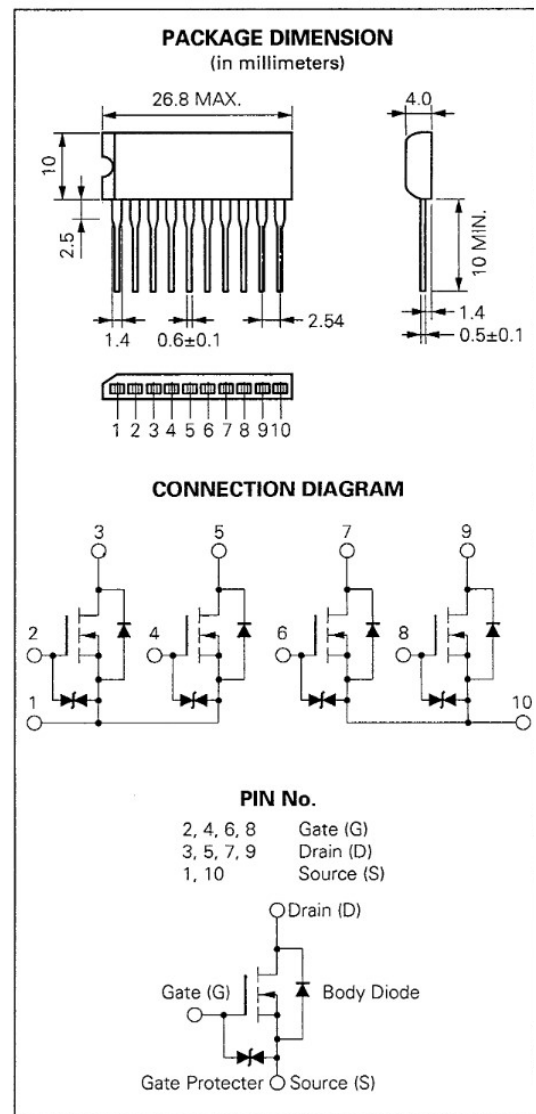
Part Number	Package	Quality Grade
μ PA1556AH	10 Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25$ °C)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage (AC)	V_{GSS}	± 20	V
Gate to Source Voltage (DC)	V_{GSS}	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	± 5.0	A/unit
Drain Current (pulse)	$I_{D(pulse)*}$	± 20	A/unit
Total Power Dissipation (4 circuits)			
< $T_c = 25$ °C>	PT_1	28	W
Total Power Dissipation (4 circuits)			
< $T_a = 25$ °C>	PT_2	3.5	W
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_j	150	°C

* $PW \leq 10 \mu s$, Duty Cycle ≤ 1 %



ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	4.0			S	V _{DS} = 10 V, I _D = 3 A
Drain to Source On-state Resistance	R _{DS(on)1}		0.20	0.25	Ω	V _{GS} = 10 V, I _D = 3 A
Drain to Source On-state Resistance	R _{DS(on)2}		0.25	0.33	Ω	V _{GS} = 4 V, I _D = 3 A
Input Capacitance	C _{iss}		700		pF	V _{DS} = 10 V V _{GS} = 0
Output Capacitance	C _{oss}		200		pF	V _{GS} = 0 f = 1.0 MHz
Reverse Transfer Capacitance	C _{rss}		30		pF	
Turn-On Delay Time	t _{d(on)}		35		ns	I _D = 3 A V _{GS} = 10 V
Rise Time	t _r		60		ns	V _{CC} = 50 V
Turn-Off Delay Time	t _{d(off)}		800		ns	R _L = 17 Ω, R _{in} = 10 Ω See Fig. 1
Fall Time	t _f		200		ns	
Total Gate Charge	Q _G		17		nC	V _{GS} = 10 V I _D = 5 A V _{DD} = 80 V
Gate to Source Charge	Q _{GS}		2.5		nC	See Fig. 2
Gate to Drain Charge	Q _{GD}		4		nC	
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 5 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		120		ns	I _F = 5 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		230		nC	di/dt = 50 A/μs

Fig. 1 Switching Time Test Circuit

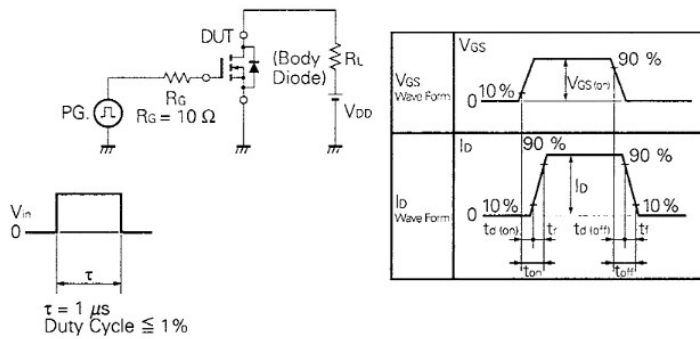
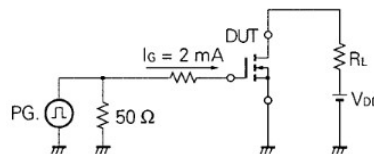
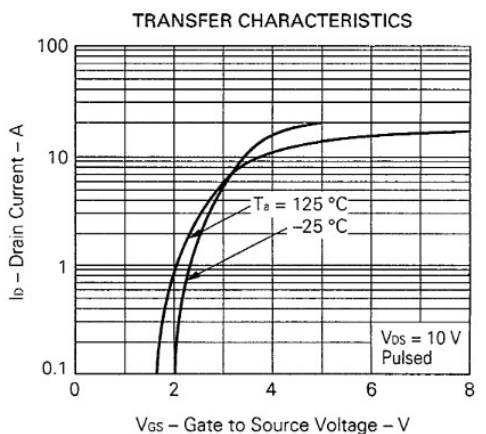
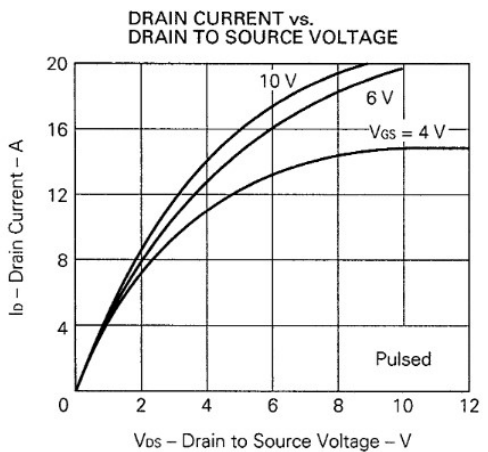
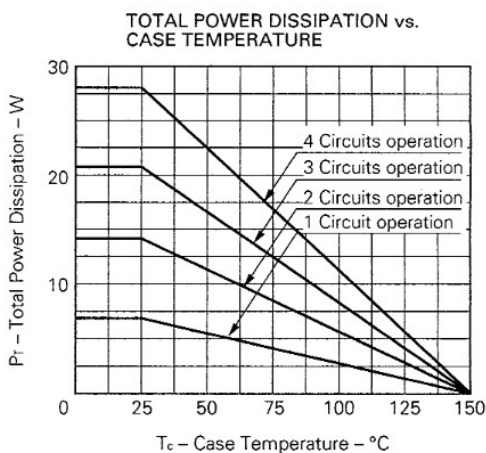
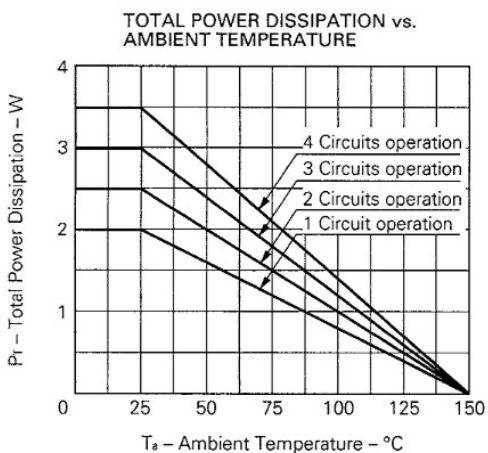
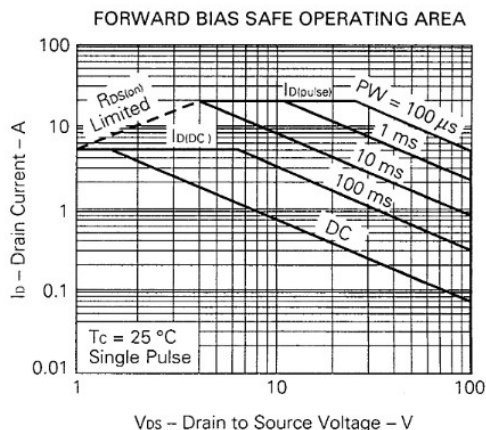
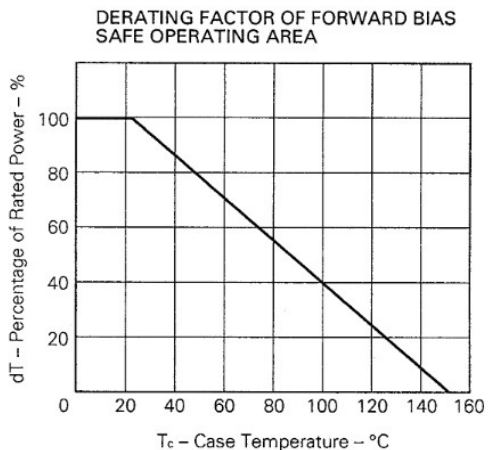
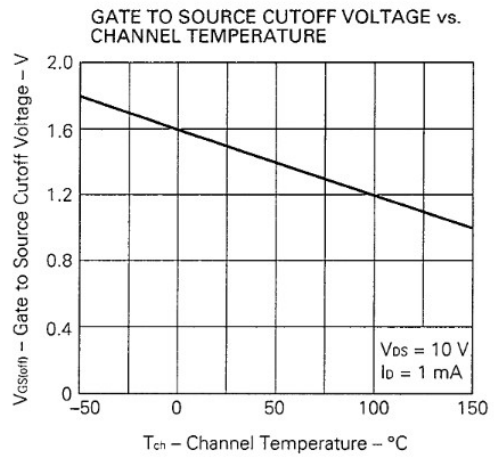
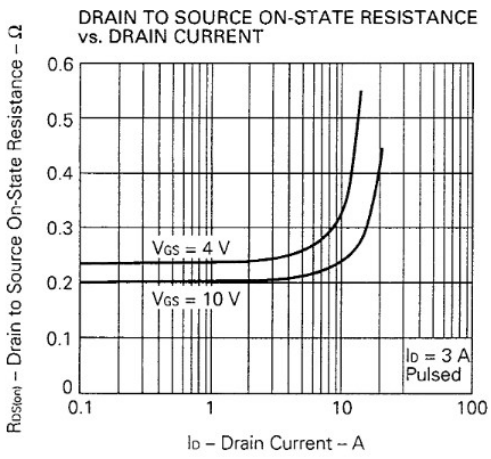
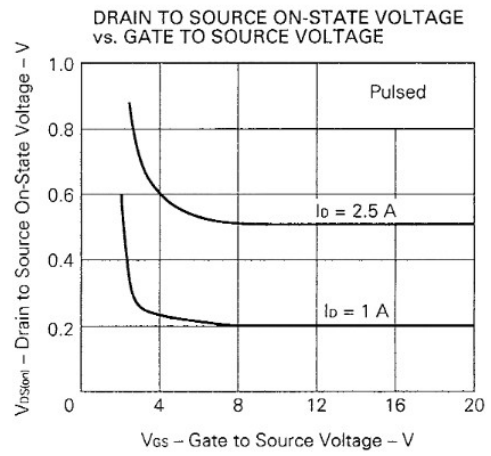
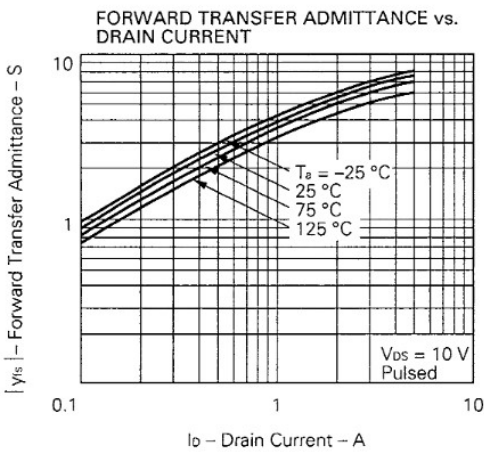
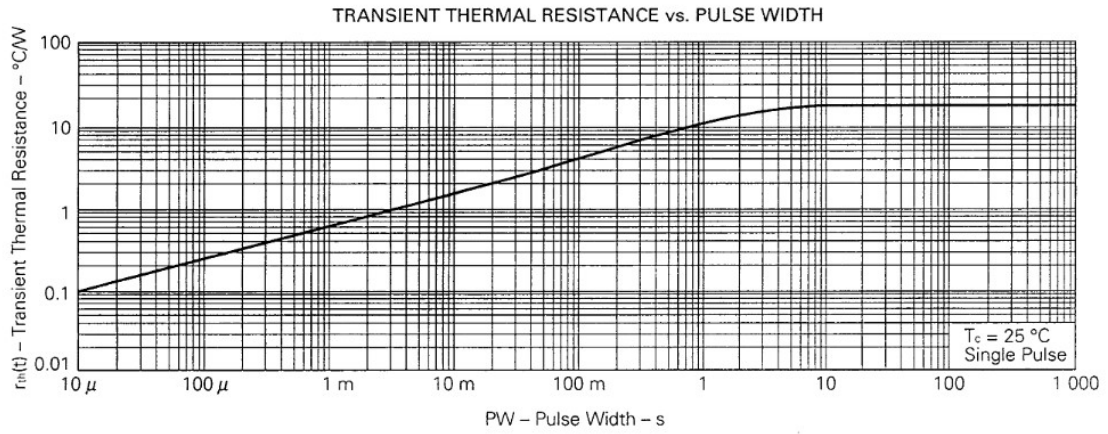


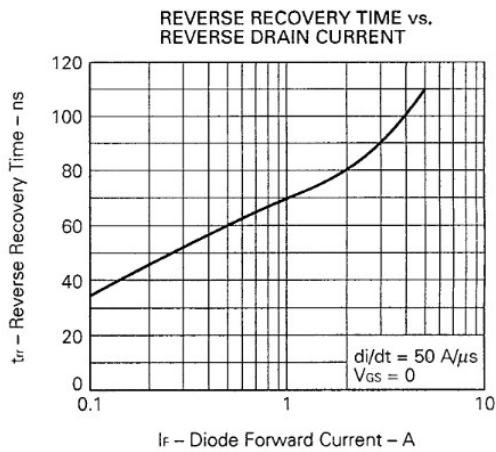
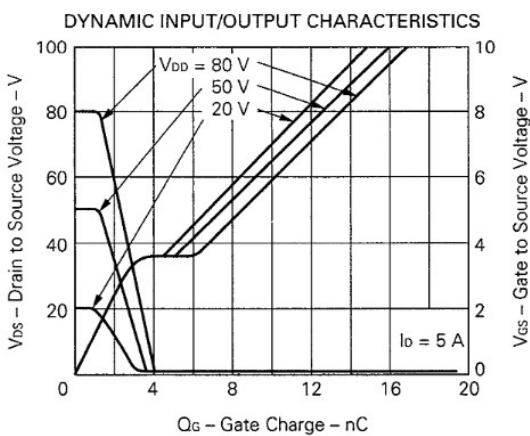
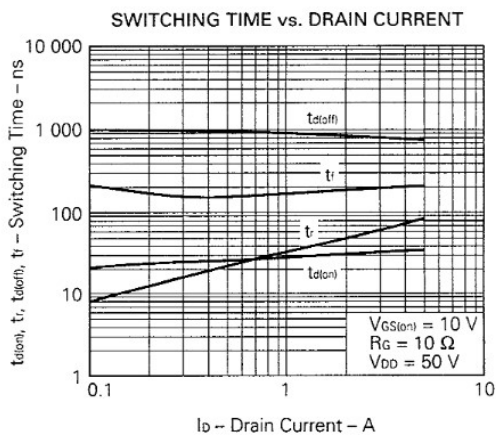
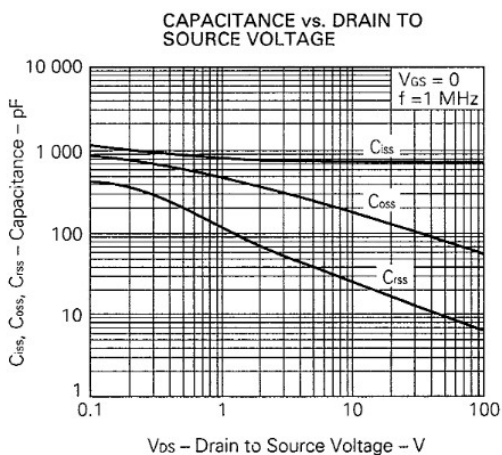
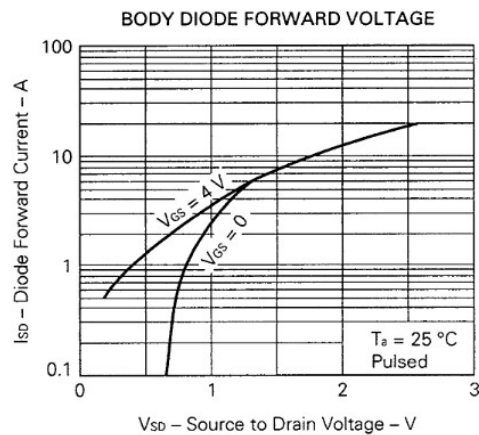
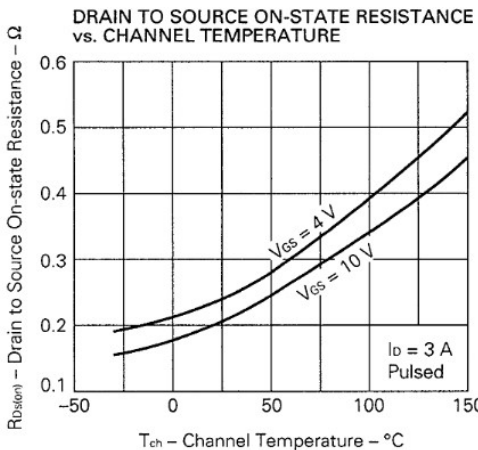
Fig. 2 Gate Charge Test Circuit



TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)







Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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