monolithic dual n-channel JFETs *designed for . . .*

Siliconix

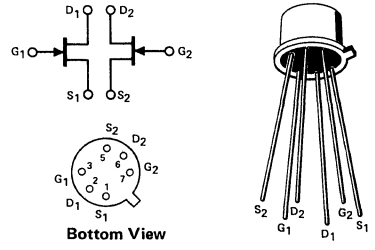
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . . 375 mW
Power Derating . . . . . 3.0 mW/°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature (1/16" from case for 10 seconds) . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U410			U411			U412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3 5	-0.5		-3 5	-0.5		-3 5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0 V, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0 5		5 0	0.5		5.0	0.5		5 0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
5	STATIC	I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	-0 2		-3.0	-0.2		-3 0	-0 2		-3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,200	600		1,200	600		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4 5			4 5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1 2			1.2			1.2		pF		f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A
2. Pulse test duration = 300 μsec, duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP