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## FSK DEMODULATOR / TONE DECODER

### ■ GENERAL DESCRIPTION

The **NJM2211** is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

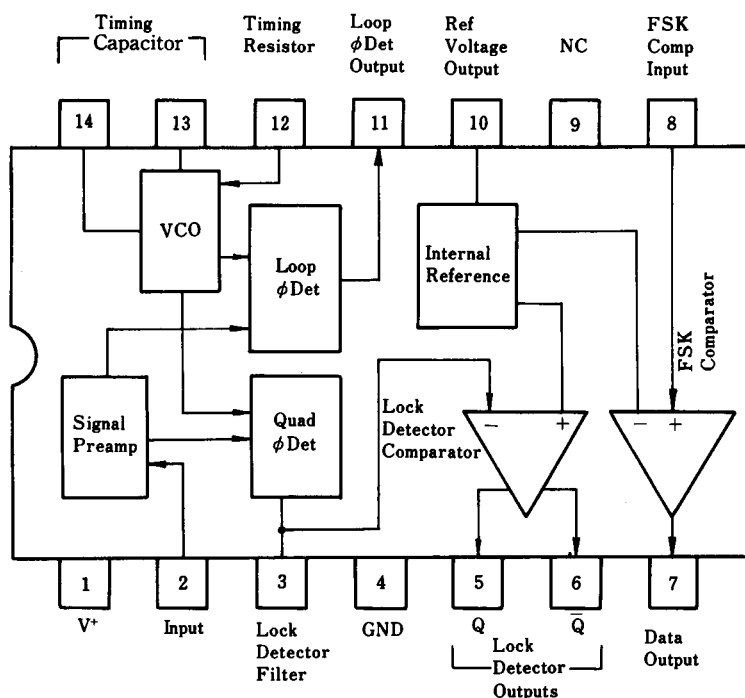
### ■ FEATURES

- Wide Operating Voltage (4.5V to 20V)
- Wide frequency range (0.01Hz to 300kHz)
- DTL / TTL / ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range (2mV to 3V<sub>rms</sub>)
- Adjustable tracking range ( $\pm 1\%$  to  $\pm 80\%$ )
- Excellent temperature stability (20ppm / °C typical)
- Package Outline DIP14, DMP14
- Bipolar Technology

### ■ APPLICATIONS

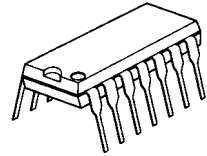
- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

### ■ PIN CONFIGURATION

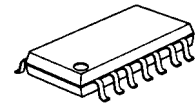


**NJM2211D**  
**NJM2211M**

### ■ PACKAGE OUTLINE



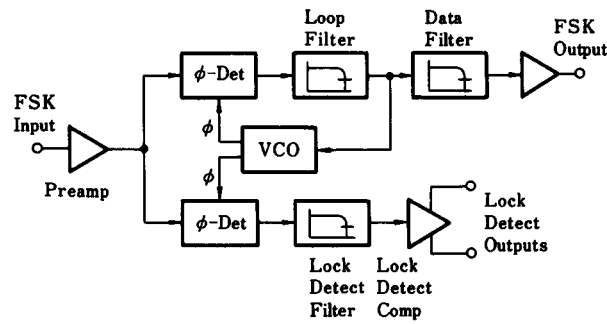
**NJM2211D**



**NJM2211M**

# NJM2211

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=25^\circ\text{C}$ )

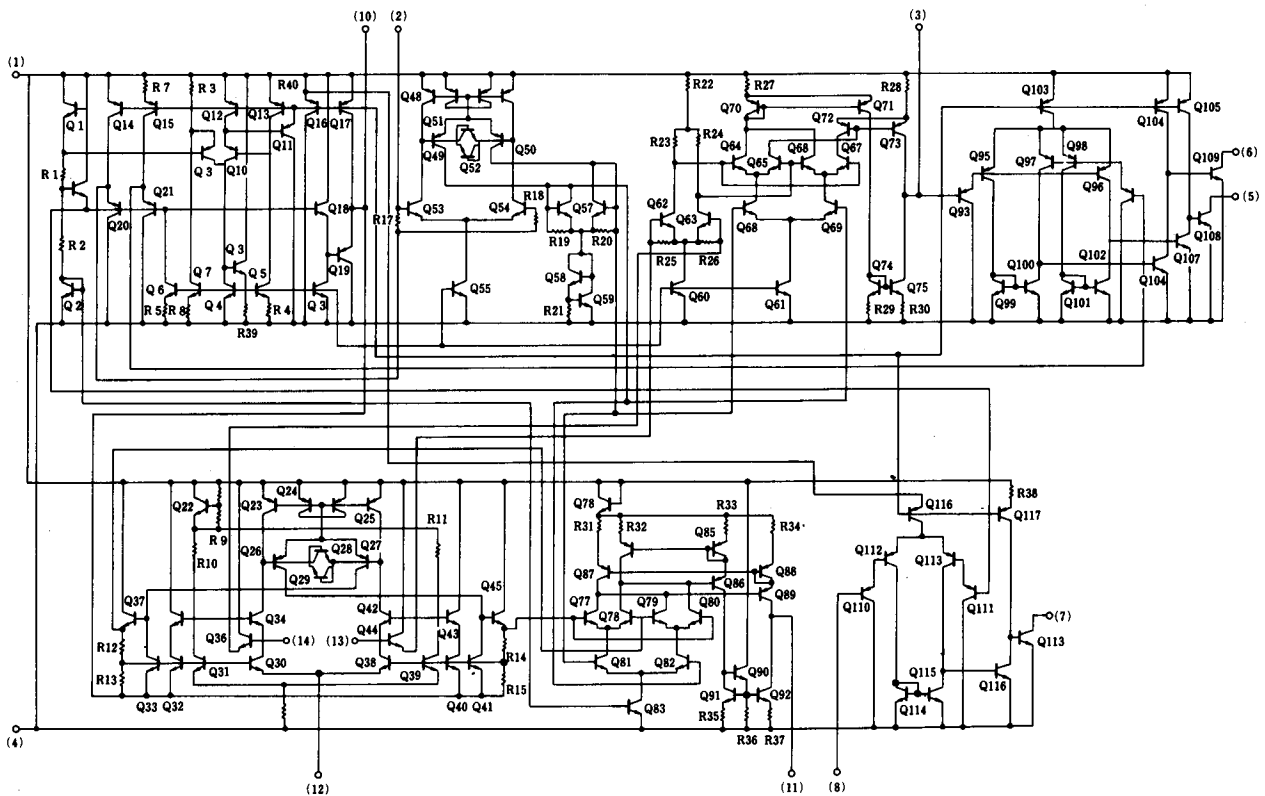
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+$	20	V
Input Signal Level	$V_{IN}$	3	Vrms
Power Dissipation	$P_D$	(DIP14) 700 (DMP14) 300	mW mW
Operating Temperature Range	$T_{opr}$	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-40 to +125	$^\circ\text{C}$

## ■ ELECTRICAL CHARACTERISTICS

( $V^+=+12V$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	$V^+$		4.5	-	20	V
Operating Current	$I_{CC}$	$R_0 \geq 10k\Omega$	-	5	11	mA
Oscillator						
Frequency Accuracy	$\Delta f_0$		-	$\pm 1.0$	-	%
Frequency Stability Temp. Coefficient	$\Delta f_0 / \Delta T$	$R_1 = \infty$	-	$\pm 20$	-	ppm / $^\circ C$
Power Supply Rejection	PSRR	$V^+ = 12 \pm 1V$ $V^+ = 5 \pm 0.5V$	-	$\pm 0.05$ $\pm 0.2$	$\pm 1.5$	% / V % / V
Upper Frequency Limit	$f_{0MAX}$	$R_0 = 8.2k\Omega$ , $C_0 = 400pF$	-	300	-	kHz
Lowest Operating Frequency	$f_{0MIN}$	$R_0 = 2M\Omega$ , $C_0 = 50\mu F$	-	0.01	-	Hz
Timing Resistor						
Timing Resistor	$R_0$	Operating Range	5	-	2000	k $\Omega$
		Recommended Range	15	-	100	k $\Omega$
Loop Phase Detector						
Peak Output Current	$I_o$	Meas. at pin 11	$\pm 100$	$\pm 200$	$\pm 300$	$\mu A$
Output Offset Current	$I_{OS}$		-	$\pm 2.0$	-	$\mu A$
Output Impedance	$Z_o$		-	1.0	-	M $\Omega$
Maximum Voltage Swing	$V_{OM}$	Ref. to pin 10	$\pm 4.0$	$\pm 5.0$	-	V
Quadrature Phase Detector						
Peak Output Current	$I_o$	Meas. at Pin 3	-	150	-	$\mu A$
Output Impedance			-	1.0	-	M $\Omega$
Maximum Voltage Swing			-	11	-	$V_{P-P}$
Input Preamp						
Input Impedance	$R_{IN}$	Meas. at Pin 2	-	20	-	k $\Omega$
Input Signal Voltage Required to Cause Limiting	$V_{IN}$		-	2	-	mVrms
Voltage Comparator						
Input Impedance	$R_{IN}$	Measure at Pin 3 & 8	-	2	-	M $\Omega$
Input Bias Current	$I_B$		-	100	-	nA
Voltage Gain	$G_V$	$R_L = 5.1k\Omega$	-	70	-	dB
Output Voltage Low	$V_{SAT}$	5, 6, 7PIN $I_C = 3mA$	-	0.3	1.0	V
Output Leakage Current	$I_{LEAK}$	$V_0 = 12V$	-	0.01	11	$\mu A$
Internal Reference						
Output Voltage	$V_{REF}$	Measure at Pin 10	4.75	5.30	5.85	V
Output Impedance	$Z_o$		-	100	-	$\Omega$

## ■ EQUIVALENT CIRCUIT



## ■ CIRCUIT FUNCTION

### ● Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20k $\Omega$ . Recommended input signal levels in the range of 10mVrms to 3Vrms.

### ● Quadrature Phase Detector Output (Pin 3)

This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of  $R_D$  and  $C_D$  (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

### ● Lock-Detect Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector type output and required a pull-up resistor,  $R_L$ , to  $V^+$  for proper operation. In the "low" state it can sink up to 5mA of load current.

### ● Lock-Detect Complement, $\bar{Q}$ (Pin 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5mA of load current in the low or "on" state.

### ● FSK Data Output (Pin 7)

This output is an open collector logic stage which requires a pull-up resistor,  $R_L$ , to  $V^+$  for proper operation. It can sink 5mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

### ● FSK Comparator Input (Pin 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by  $R_F$  and  $C_F$  of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage,  $V_R$ , available at pin 10.

● **Reference Voltage  $V_R$  (Pin 10)**

This pin is internally biased at the reference voltage level,  $V_R$ ;  $V_R = V^+ / 2 - 650\text{mV}$ . The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11, and 12. Pin 10 must be bypassed to ground with a  $0.1\mu\text{F}$  capacitor.

● **Loop Phase Detector Output (Pin 11)**

This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by  $R_1$  and  $C_1$  connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to  $V_{REF}$ . The peak voltage swing available at the phase detector output is equal to  $\pm V_{REF}$ .

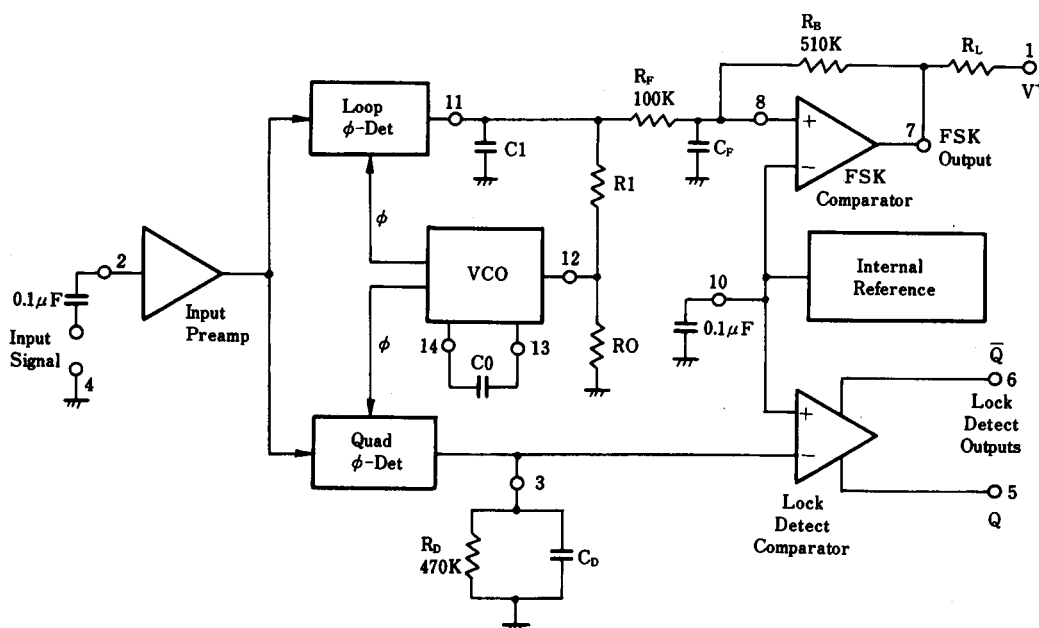


Figure 1. FSK & Tone Detection

● **VCO Control Input (Pin 12)**

VCO free-running frequency is determined by external timing resistor,  $R_0$ , connected from this terminal to ground. The VCO free-running frequency,  $f_0$ , is given by :

$$f_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

where  $C_0$  is the timing capacitor across pins 13 and 14. For optimum temperature stability  $R_0$  must be in the range of  $10\text{k}\Omega$  to  $100\text{k}\Omega$  (see Typical Electrical Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to  $V_R$ . The maximum timing current drawn from pin 12 must be limited to  $\leq 3\text{mA}$  for proper operation of the circuit.

● **VCO Timing Capacitor (Pins 13 and 14)**

VCO frequency is inversely proportional to the external timing capacitor,  $C_0$ , connected across these terminals.  $C_0$  must be non-polarized, and in the range of  $200\text{pF}$  to  $10\mu\text{F}$ .

● **VCO Frequency Adjustment**

VCO can be fine tuned by connecting a potentiometer,  $R_x$ , in series with  $R_0$  at pin 12 (see Figure 2)

● **VCO Free-Running Frequency,  $F_0$**

The **NJM2211** does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with  $C_D$  disconnected) with no input and also pin 2 shorted to pin 10.

## ■ DESIGN EQUATIONS

See Figure 1 for Definitions of Components.

1. VCO Center Frequency,  $f_0$  :

$$f_0(\text{Hz}) = \frac{1}{R_0 C_0}$$

2. Internal Reference Voltage,  $V_R$  (measured at pin 10) :

$$V_R = \left( \frac{+V_S}{2} \right) - 650\text{mV}$$

3. Loop Lowpass Filter Time Constant,  $\tau$  :

$$\tau = R_1 C_1$$

4. Loop Damping,  $\xi$  :

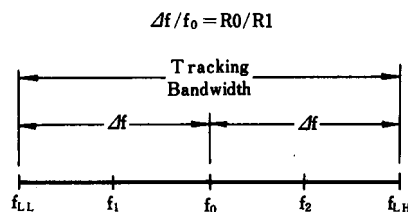
$$\xi = \left( \sqrt{\frac{C_0}{C_1}} \right) \left( \frac{1}{4} \right)$$

5. Loop Tracking Bandwidth,  $\pm\Delta f/f_0$  :

$$\Delta f/f_0 = R_0 / R_1$$

6. FSK Data Filter Time Constant,  $T_F$  :

$$T_F = R_F C_F$$



7. Loop Phase Detector Conversion Gain,  $K_\phi$  :

( $K_\phi$  is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input) :

$$K_\phi \text{ (in volts per radian)} = \frac{(-2)(V_{REF})}{\pi}$$

8. VCO conversion Gain,  $K_0$ , is the amount of change in VCO frequency per unit of DC voltage change at pin 11 :

$$K_0 \text{ (in Hertz per volt)} = \frac{-1}{C_0 R_1 V_{REF}}$$

9. Total Loop Gain  $K_T$  :

$$K_T \text{ (in radians per second per volt)} = 2\pi K_\phi K_0 = 4 / C_0 R_1$$

10. Peak Phase-Detector Current,  $I_A$  :

$$I_A \text{ (mA)} = \frac{V_{REF}}{25}$$

## ■ APPLICATIONS

### FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows : R<sub>0</sub> and C<sub>0</sub> set the PLL center frequency. R<sub>1</sub> sets the system bandwidth, and C<sub>1</sub> sets the loop filter time constant and the loop damping factor. C<sub>F</sub> and R<sub>F</sub> form a one pole post-detection filter for the FSK data output. The resistor R<sub>B</sub> (=510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

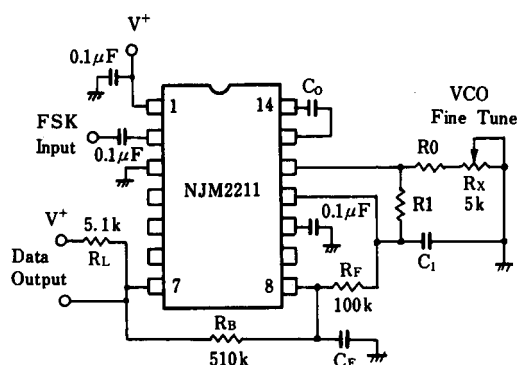


Figure 2. FSK Decoding

Table 1. Recommended Value for FSK

(Ref. Fig. 2)

FSK Band	Component Values
300 Band F <sub>1</sub> =1070Hz f <sub>2</sub> =1270Hz	C <sub>0</sub> =0.039µF C <sub>F</sub> =0.005µF C <sub>1</sub> =0.01µF R <sub>0</sub> =18kΩ R <sub>1</sub> =100kΩ
300 Band f <sub>1</sub> =2025Hz f <sub>2</sub> =2225Hz	C <sub>0</sub> =0.022µF C <sub>F</sub> =0.005µF C <sub>1</sub> =0.0047µF R <sub>0</sub> =18kΩ R <sub>1</sub> =200kΩ
1200 Band f <sub>1</sub> =1200Hz f <sub>2</sub> =2200Hz	C <sub>0</sub> =0.027µF C <sub>F</sub> =0.0022µF C <sub>1</sub> =0.01µF R <sub>0</sub> =18kΩ R <sub>1</sub> =30kΩ

### Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components ; R<sub>0</sub>, R<sub>1</sub>, C<sub>0</sub>, C<sub>1</sub> and C<sub>F</sub>. For a given set of FSK mark and space frequencies. f<sub>1</sub> and f<sub>2</sub>, these parameters can be calculated as follows :

1. Calculate PLL center frequency, f<sub>0</sub>

$$f_0 = \frac{f_1 + f_2}{2}$$

2. Chose a value of timing resistor R<sub>0</sub> to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. The recommended value is R<sub>0</sub> ≅ 20kΩ. The final value of R<sub>0</sub> is normally fine-tuned with the series potentiometer, R<sub>x</sub>.

3. Calculate value of C<sub>0</sub> from Design Equation No.1 or from Typical Performance Characteristics :

$$C_0 = 1 / R_0 f_0$$

4. Calculate R<sub>1</sub> to give a Δf equal to the mark-space deviation :

$$R_1 = R_0 [f_0 / (f_1 - f_2)]$$

5. Calculate C<sub>1</sub> to set loop damping. (See Design Equation No.4.)

Normally, ξ ≈ 1 / 2 is recommended

$$\text{Then : } C_1 = C_0 / 4 \text{ for } \xi = 1 / 2$$

6. Calculate Data Filter Capacitance, C<sub>F</sub> :

For R<sub>F</sub>=100kΩ. R<sub>B</sub>=510kΩ, the recommended value of C<sub>F</sub> is :

$$C_F (\text{in } \mu\text{F}) = \frac{3}{\text{Band Rate}}$$

Note : All calculated component values except R<sub>0</sub> can be rounded off to the nearest standard value, and R<sub>0</sub> can be varied to fine-tune center frequency through a series potentiometer, R<sub>x</sub> (see Figure 2).



# NJM2211

## Design Example

75 Band FSK demodulator with mark / space frequencies of 1110 / 1170Hz :

Step 1 : Calculate  $f_0$  :

$$f_0 = (1110 + 1170) (1 / 2) = 1140\text{Hz}$$

Step 2 : Choose  $R_0 = 20\text{k}\Omega$  (18k $\Omega$  fixed resistor in series with 5k $\Omega$  potentiometer)

Step 3 : Calculate  $C_0$  from VCO Frequency vs. Timing Capacitor :  $C_0 = 0.044\mu\text{F}$

Step 4 : Calculate  $R_1$  :  $R_1 = R_0 (1140 / 60) = 380\text{k}\Omega$

Step 5 : Calculate  $C_1$  :  $C_1 = C_0 / 4 = 0.011\mu\text{F}$

Note : All values except  $R_0$  can be rounded off to nearest standard value.

## FSK Decoding With Carrier Detect

The lock-detect section of the **NJM2211** can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.

The Minimum value of the lock-detect filter capacitance  $C_D$  is inversely proportional to the capture range,  $\pm\Delta f_c$ . This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by  $C_1$ . For most applications,  $\Delta f_c < \Delta f / 2$ , For  $R_D = 470\text{k}\Omega$ , the approximate minimum value of  $C_D$  can be determined by :

$$C_D (\mu\text{F}) \geq 16 / \text{capture range in Hz}$$

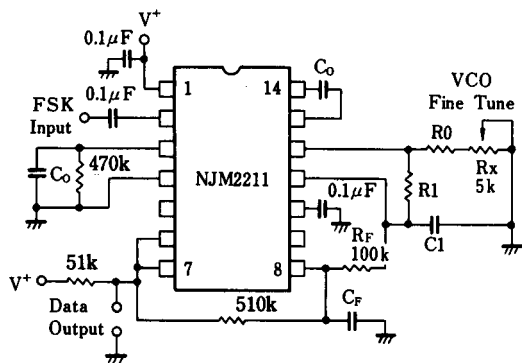
With values of  $C_D$  that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of  $C_D$  will slow the response time of the lock-detect output.

## Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and  $\bar{Q}$  at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors  $R_{L1}$  and  $R_{L2}$  as shown in Figure 4.

With reference to Figure 1 and 4, the function of the external circuit components can be explained as follows :  $R_0$  and  $C_0$  set VCO center frequency,  $R_1$  sets the detection bandwidth,  $C_1$  sets the lowpass-loop filter time constant and the loop damping factor, and  $R_{L1}$  and  $R_{L2}$  are the respective pull-up resistors for the Q and  $\bar{Q}$  logic outputs.



(Data Output is "low" when no carrier is present)

Figure 3. FSK Demodulation with Carrier Detect Capability

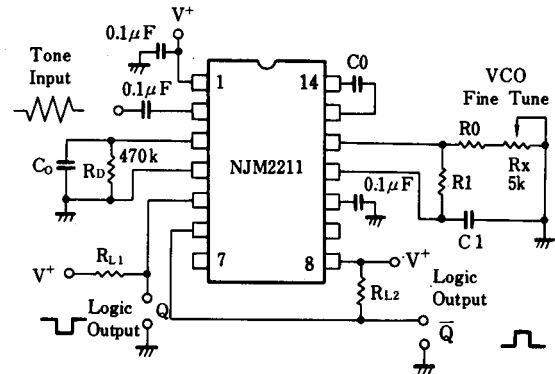


Figure 4. Tone Detection

## Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components : R0, R1, C0, C1, and C<sub>D</sub>. For a given input tone frequency, f<sub>s</sub>, these parameters are calculated as follows :

1. Choose R0 to be in the range of 15kΩ to 100kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f<sub>0</sub> equal to f<sub>s</sub> : C0=1 / R0f<sub>s</sub>.
3. Calculate R1 to set bandwidth ±Δf (see Design Equation No.5) : R1=R0 (f<sub>0</sub> / Δf)

Note : The total detection bandwidth covers the frequency range of f<sub>0</sub>=Δf

4. Calculate value of C1 for a given loop damping factor :

$$C1 = C0 / 16\xi^2$$

Normally  $\xi \approx 1 / 2$  is optimum for most tone-detector applications, giving C1=0.25 C0.

Increasing C1 improves the out-of band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor C<sub>D</sub>. To avoid chatter at the logic output, with R<sub>D</sub>=470kΩ, C<sub>D</sub> must be :

$$C_D (\mu F) \geq (16 / \text{capture range in Hz})$$

Increasing C<sub>D</sub> slows the logic output response time.

## Design Examples

Tone detector with a detection band of 1kHz±20Hz :

Step 1 : Choose R0=20kΩ (18kΩ in series with 5kΩ potentiometer).

Step 2 : Choose C0 for f<sub>0</sub>=1kHz : C0 =0.05μF.

Step 3 : Calculate R1 : R1=(R0)(1000 / 20)=1MΩ.

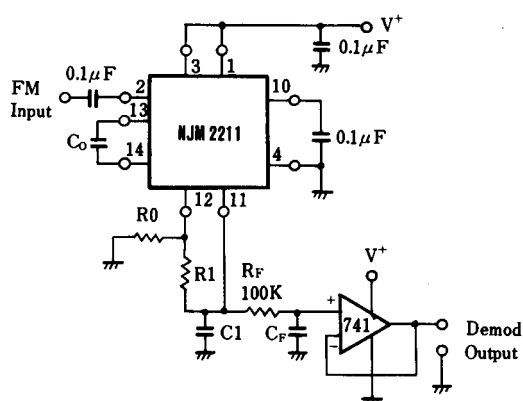
Step 4 : Calculate C1 : for  $\xi=1 / 2$ , C1=0.25μF, C2=0.013μF.

Step 5 : Calculate C<sub>D</sub> : C<sub>D</sub>=16 / 38=0.42μF.

Step 6 : Fine tune the center frequency with the 5kΩ potentiometer, R<sub>x</sub>.

## Linear FM Detection

The **NJM2211** can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R<sub>F</sub> and C<sub>F</sub>, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.



**Figure 5. Linear FM Detector**

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as :

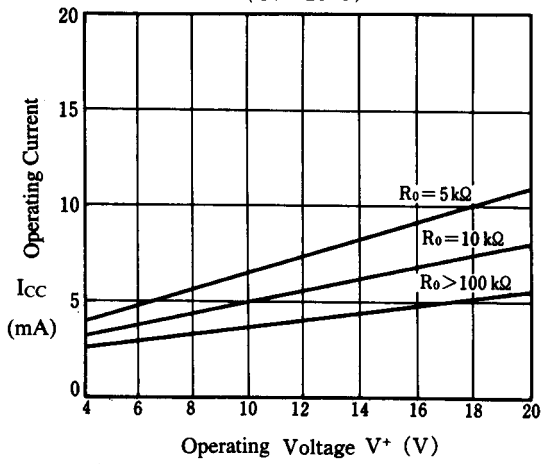
$$V_{OUT} = R1 V_R / 100 R0 \text{ Volts/\% deviation}$$

where V<sub>R</sub> is the internal reference voltage. For the choice of extremal components R1, R0, C<sub>D</sub>, C1 and C<sub>F</sub>, see the section on Design Equations.

## ■ TYPICAL CHARACTERISTICS

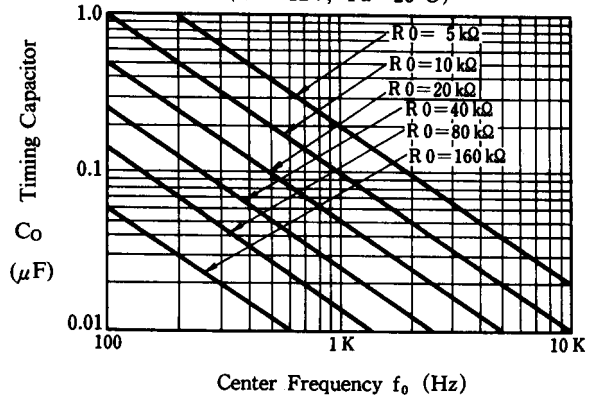
### Operating Current

( $T_a = 25^\circ\text{C}$ )



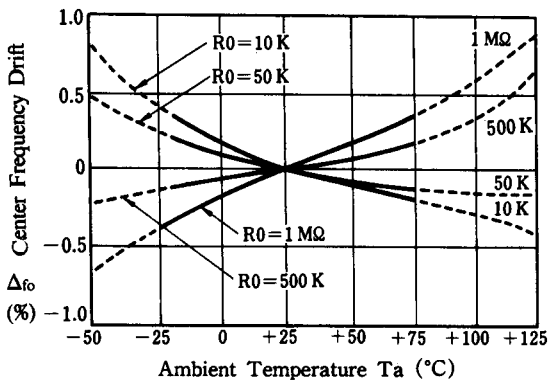
### VCO Frequency

( $V^+ = 12\text{V}$ ,  $T_a = 25^\circ\text{C}$ )



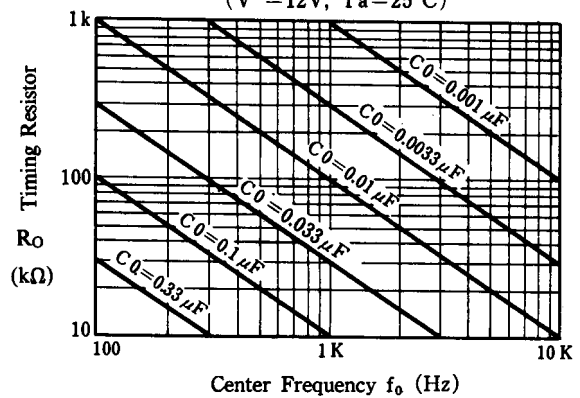
### Center Frequency Drift

( $V^+ = 12\text{V}$ ,  $R_1 = 10R_0$ ,  $f = 1\text{kHz}$ )



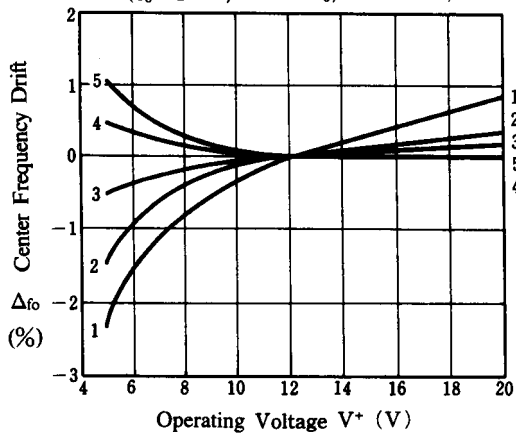
### VCO Frequency

( $V^+ = 12\text{V}$ ,  $T_a = 25^\circ\text{C}$ )



### Center Frequency

( $f_0 = 1\text{kHz}$ ,  $R \geq 10R_0$ ,  $T_a = 25^\circ\text{C}$ )



Curve	$R_0$
1	5 K
2	10 K
3	30 K
4	100 K
5	300 K

#### [CAUTION]

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