MM5382, MM5383 digital calendar clock radio circuits

general description

The MM5382 and MM5383 digital calendar clock circuits provide the timing, control, and interface circuitry for a minimum-cost, solid state, digital clock radio.

The timekeeping function operates in either a 12-hour or a 24-hour mode. The MM5382 is the 12-hour version, and has a month-date format; the MM5383 is the 24-hour version, and has a date-month format.

Outputs consist of a presettable 59-minute sleep timer (e.g., a timed radio turn-off) and an alarm tone. A power failure indication warns the user that the time displayed may be in error.

Other features include: alarm display; brightness control; 24-hour alarm set; PM indication; fast and slow set controls; and a 9-minute snooze alarm. (The MM5383 has an alarm "ON" indicator.) Both circuits provide open drain outputs for the direct drive of LED displays to 15 mA.

features

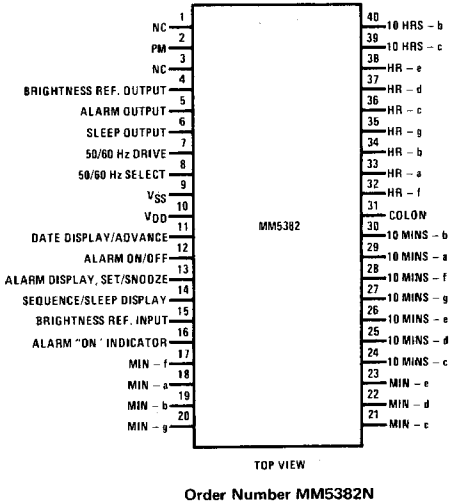
- 50 or 60 Hz operation
- 12 hour, month-date (MM5382) or 24 hour, date-month (MM5383) display
- PM indication (MM5382)
- Leading zero blanking
- 24-hour alarm setting
- Power failure indication (the word "OFF" is displayed in MM5382 and all "ON" digits blink in MM5383
- Brightness control
- Date display (4 year calendar)
- Presettable 59-minute sleep timer
- Alarm display
- Fast and slow set sleep and alarm
- 9 minute snooze alarm
- Blinking colon
- Alarm "ON" indication (MM5382 only)
- Alarm tone output
- No illegal time or date display at turn-on

applications

- Alarm clock
- Desk clock
- Clock radios
- Stop watch
- Industrial clock
- Portable clock
- Timer
- Sequential controllers

connection diagrams

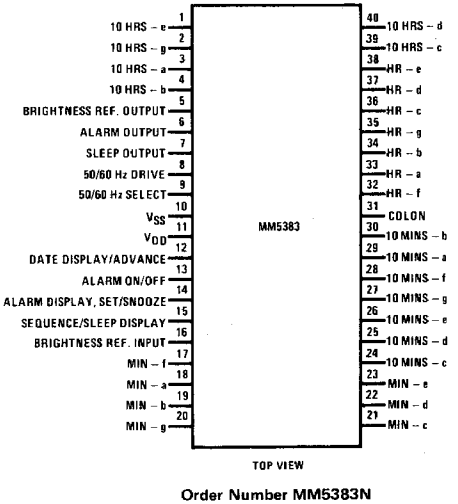
Dual-In-Line Package



TOP VIEW

Order Number MM5382N
See Package 24

Dual-In-Line Package



TOP VIEW

Order Number MM5383N
See Package 24

FIGURE 1

absolute maximum ratings

Voltage at Any Pin except Segment, Colon, and PM	V_{SS} +0.3V to V_{SS} −28V
Voltage at Segment, Colon, and PM	V_{SS} +0.3V to V_{SS} −10V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation	1 Watt
Electrical Characteristics	
T_A within Operating Range	V_{SS} = +18V to +26V, V_{DD} = 0V, with specified output drive unless otherwise specified
Functional Clock Voltage	V_{SS} = +8V to +26V, V_{DD} = 0 (No output drive spec)

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	No output levels				
	V_{SS} = 8V			4	mA
	V_{SS} = 26V			5	mA
50/60 Hz Input					
Frequency		DC	50 or 60	30k	Hz
Voltage	V_{SS} = 18V				
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	
Switch Input Voltages (Date, Sequence, Alarm Enable, Alarm Display)					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level (1)	Nominal Floating Level	V_{SS}−3	Float	V_{SS}−6	V
Logical Low Level (2)		V_{DD}	V_{DD}	V_{DD}+2	V
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level	Internal Depletion Load to V_{DD}			V_{SS}−15	
Power Failure Detect Voltages	(V_{SS} Voltage)	1.0		8.0	V
Output Currents:	V_{SS} = 18V to 26V, V_{DD} = 0V				
All Segments and Colon					
Logical High Level, Source	V_{OH} = V_{SS} −2V	15			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} −10V			10	μA
PM Indicator and Alarm Indicator					
Logical High Level, Source	V_{OH} = V_{SS} −2V	15			mA
Logical Low Level, Leakage	V_{OH} = V_{SS} −10V			10	μA
Alarm and Sleep Outputs					
Logical High Level, Source	V_{OH} = V_{SS} −2V	2			mA
Logical Low Level, Sink	V_{OH} = V_{SS} −15V	500			μA
Alarm Output Tone Frequency Modulated with 2 Hz	V_{SS} = 18V to 26V	400		2000	Hz
Total Power Dissipation	V_{SS} = 26V, V_{DD} = 0V I_{OUT} (25 Segments) = 15 mA T = 70°C V_{OUT} = V_{SS} −2V			830	mW

block diagram

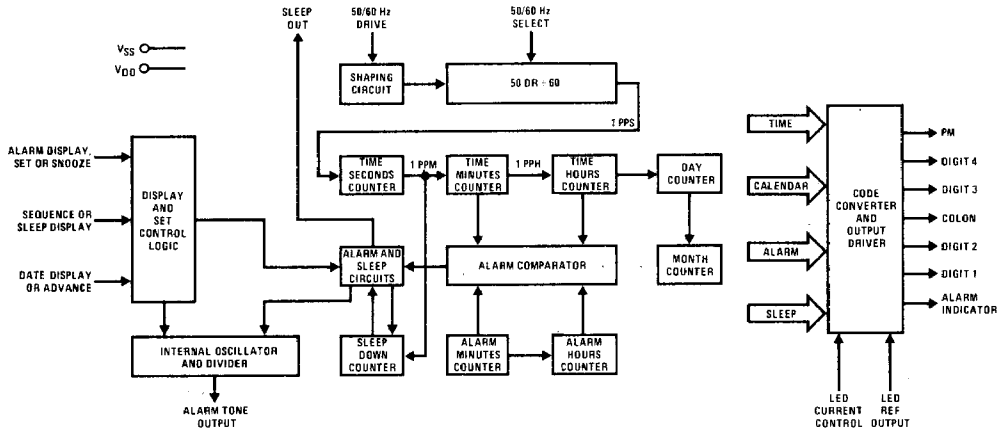


FIGURE 2.

TABLE I. Display Modes and Setting Control Functions

FUNCTION	STEP	DATE DISPLAY/ ADVANCE	ALARM DISPLAY – SET/SNOOZE	SEQUENCE/SLEEP DISPLAY
Display Time	1	Float	Float	Float
Set Time	1	Float	Float	Momentary connect to V_{DD} for each step of setting time and calendar
	2	V_{DD}	Float	Float
Display Alarm	1	Float	Connect to V_{DD} for < 2 seconds	Float
Set Alarm:				
2 Hz Rate	1	Float	Connect to V_{DD} for > 2 seconds	Float
60 Hz Rate	2	V_{DD}	V_{DD}	Float
Display Sleep	1	Float	Float	Connect to V_{SS} for < 2 seconds
Set Sleep:				
2 Hz Rate	1	Float	Float	Hold V_{SS} for > 2 seconds (Advances at 2 Hz Rate)
60 Hz Rate	2	V_{DD} (Advances at 60 Hz Rate)	Float	V_{SS}

functional description

Connection diagrams for the MM5382 and the MM5383 Digital Clock Radio Circuits are shown in *Figure 1*. A block diagram of these devices is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 2*. *Figure 3* shows the general purpose alarm clock and procedure to set the time, month, day, alarm and sleep counters. Table I shows the display modes and setting control functions.

50 or 60 Hz Drive: A shaping circuit is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 4V of hysteresis. A simple RC filter should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz base. This counter is programmed to divide by 60 simply by leaving the pin unconnected; a pull-down to V_{DD} is provided by an internal resistor. Operation at 50 Hz is programmed by connecting this input to V_{SS}.

Alarm Operation: The internal alarm comparator senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The alarm latch remains set for 59 minutes during which time the alarm or radio will sound if the latch outputs are not temporarily inhibited by another latch set by the snooze input or reset by the alarm "OFF" input.

functional description (Continued)

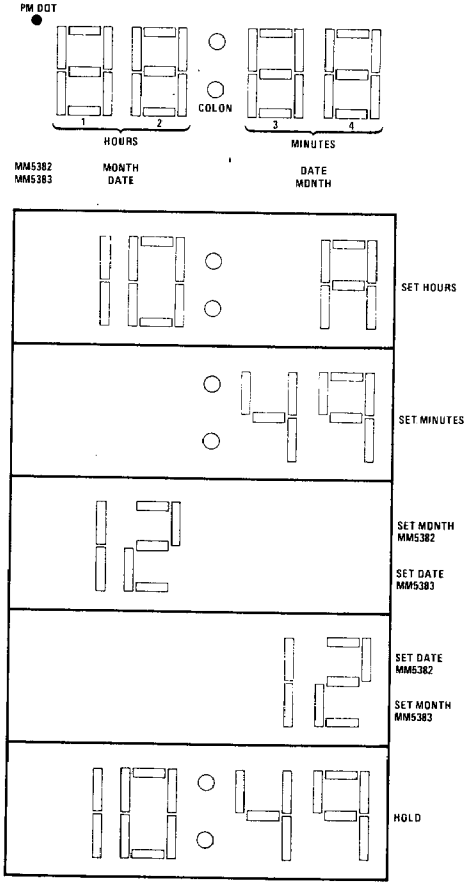
Alarm ON/OFF/RADIO Input: Momentarily leaving this input unconnected resets the alarm latch and thereby silences the alarm. This input is also used to determine if the alarm or the sleep output will be enabled when the alarm latch is set. By connecting the input pin to V_{DD}, both the alarm output and the sleep output (radio) are enabled when the alarm latch is set. If the input pin is connected to V_{SS}, only the sleep output (radio) is enabled when the alarm latch is set. Momentarily leaving this pin unconnected also readies the alarm latch for the next comparator output, hence, the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the Alarm ON/OFF Radio input pin should remain unconnected.

Alarm Output: The alarm output signal is a tone of from 400 Hz to 2000 Hz, which is gated on and off at a 2 Hz rate.

Alarm Display, Set/Snooze: Momentarily connecting this pin to V_{DD} when the alarm and sleep outputs are disabled displays the alarm setting for 1.5 to 2 seconds. The display shows the hours and minutes of the alarm setting, a constant colon and a PM indication if the clock is in the 12 hour mode. If the input pin is held to V_{DD} for longer than 2 seconds, the minutes of the alarm counter start to advance at a 2 Hz rate. To increase the rate that the alarm counter is set at, also connect the Date/Advance input pin to V_{DD}. The minutes of the alarm counter will now advance at a 60 Hz rate. By momentarily connecting the input pin to V_{DD} when the alarm or sleep output is enabled, snooze is enabled for 8 or 9 minutes. Snooze inhibits the alarm output for between 8 and 9 minutes, after which the alarm output is enabled again. Snooze has no effect on the sleep output. The snooze feature may be repeatedly used during the 59 minutes in which the alarm latch remains set. Momentarily connecting this input pin to V_{DD} when the clock is in the power failure mode stops all power failure indications and displays alarm. If this pin is connected to V_{SS} and date advance pin is connected to V_{SS}, the clock is in a test mode. All outputs are enabled and time and alarm are set to 12:00 AM, the date is set to the 12th month and the 1st day, and the sleep counter is set to 00 minutes. If the Alarm Display, Set/Snooze is at V_{SS}, all outputs and inputs are disabled except 50/60 Hz Select and 50/60 Hz Drive.

Sleep Timer and Output: The sleep output can be used to turn off a radio after a desired interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode and setting the desired time interval. This automatically results in a current-source output, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary V_{DD} connection to the Alarm Display, Set/Snooze input.

Sequence/Sleep Display and Set: If left open, time or the counter to be set is displayed. Momentarily connecting this pin to V_{SS} displays the sleep counter for 1.5 to 2 seconds. If after 2 seconds the pin is still at V_{SS}, the sleep counter will decrement at a 2 Hz rate. To increase the rate at which the sleep counter is decremented, also connect the Date/Advance pin to VDD. The sleep counter will now decrement at a 60 Hz rate. Momentarily connecting the Sequence pin to V_{DD} steps the clock through its set modes. There are 6 states; they are real time, set hours, set minutes, set month (12 hour mode), set day (12 hour mode), and the holding state. When real time is displayed, a momentary connection to V_{DD} advances the clock to the set hours state. In this state, hours are displayed, minutes are blanked, the colon is constant, and an A or P is displayed in the unit minutes position if the clock is in the 12 hour mode. To set hours, the Date/Advance pin is connected to V_{DD}. The next time the Sequence pin is connected to V_{DD}, the clock is advanced to the set minutes state. In this state, the minutes are displayed, the hours are blank, the colon is constant and the PM indication is displayed if the clock is in the 12 hour mode and set for PM. The next state the clock advances to is the set left state. In the 12 hour mode, this is a month set state. For the 24 hour mode, this is a day set state. In this state, the left two digits of the display are shown, the colon and the right two digits of the display are blank. The next state the clock advances to is the set right state. In this state, the day in the 12 hour mode or month in the 24 hour mode is displayed in the right two digits of the display.



Time and Date Display Format in 'Set' Mode

functional description (Continued)

The left two digits and colon are blank. The next transition on the Sequence input displays real time if the minutes were not set. If the minutes counter was set, the next state the clock advances to is the holding state. In this state the time and the colon are blinking at a 2 Hz rate and held to the set time. To leave the holding state, the Sequence Input is connected to V_{DD} momentarily. If the clock remains in any state except the holding state for more than 10 seconds without being set, the clock will automatically advance to real time or the holding state if minutes were set.

Note: Time set mode should not be initiated while in alarm or sleep display 2 second time out. Time set mode should be sequenced only when the clock displays real time.

Date/Advance Input: If left open, this input has no effect on the clock. Momentarily connecting this pin to V_{DD} displays the date for 1.5 to 2 seconds if the clock was not in a set state. If after 2 seconds the input pin is still at V_{DD}, the date remains displayed until the input pin is released. If the Date/Advance pin is connected to V_{DD} when the clock is in a set mode, the counter displayed will advance at a 2 Hz rate until the pin is released. Connecting this input pin to V_{DD} when the sleep counter or the alarm counter is displayed advances the displayed counter at a 60 Hz rate. If the Date/Advance pin is connected to V_{SS}, the seconds counter is bypassed and minutes counter advances at a 1 Hz rate.

Colon: The colon output blinks at a 1 Hz rate in the run mode. It is constant during set hours and minutes, and alarm display. The colon is blank for date display. The colon blinks at a 2 Hz rate in the holding state.

Alarm Indication Output: Whenever the alarm is enabled, the Alarm Indicator output is turned on. It is used to indicate to the user that the alarm has been set.

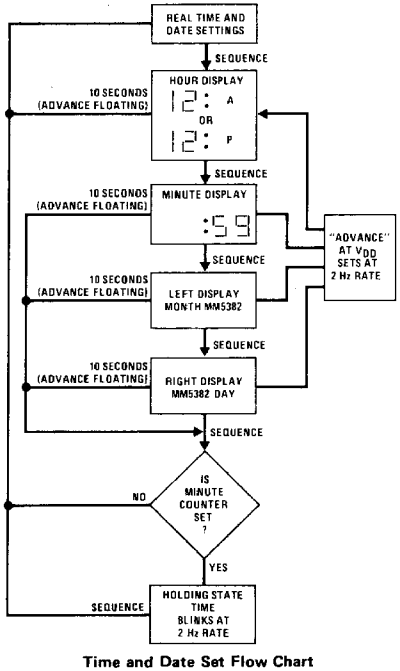
PM Output: The PM Output is available only in the MM5382. This output is enabled only when time or alarm are displayed.

Power Failure Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of the correct time, in the MM5382 the word 'OFF' is displayed blinking at a 2 Hz rate, in the MM5383 all the 'ON' segments blink at 2 Hz rate and the colon is blank. Momentarily connecting the Alarm Display Set/Snooze input to V_{DD} displays first the alarm for 1.5 to 2 seconds and then real time. In addition, if the alarm was "ON" the Alarm "ON/OFF" input should also be momentarily connected to V_{DD}.

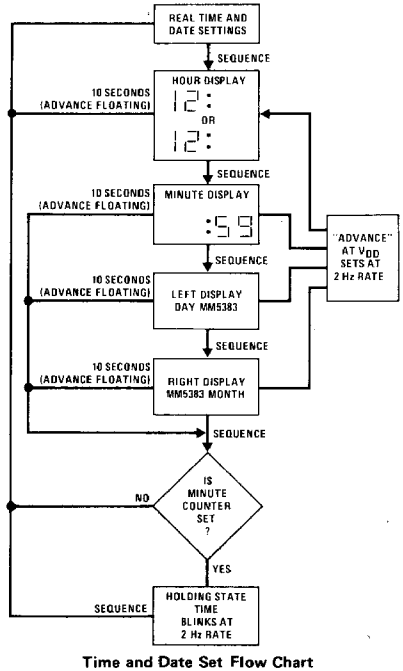
LED CURRENT CONTROL INPUT AND REFERENCE OUTPUT

Pin (15) MM5382, pin (16) MM5383 controls the gate voltage at all the display outputs and the reference device. The output drives can be disabled by connecting pin 15 MM5382, 16 MM5383 to V_{SS}. This wire-OR capability allows the display to be used for other functions (e.g., temperature). The output current can be controlled two ways; 1) driving the output in saturated mode; 2) driving the output in linear mode. (Refer to *Figures 4* and *5.*)

1. The reference device pins (4, 15) MM5382 (5, 16) MM5383 are connected as diodes and an external resistor is used to set the desired current in these diodes (see *Figure 4*). The segment drivers of all digits are connected as current mirrors. The drain



Time and Date Set Flow Chart
MM5382, 12-Hour Mode



Time and Date Set Flow Chart
MM5383, 24-Hour Mode

functional description (Continued)

voltage V1 of the segment drivers is selected such that these devices operate in saturation mode. Since the drain current variation in saturation mode operation of the MOS device is relatively constant, the segment drive current does not vary significantly, even though V1 is increased considerably. However, as the voltage across the output buffers increases, average power dissipation also increases linearly. This technique of current control is recommended to be used only with low current LEDs (1–7 mA).

2. The high current drive requirement of large LED displays can be accomplished by operating the segment drivers in the linear mode. The circuit for high current LED drivers is shown in *Figure 5*. The reference output device is used in series with a reference LED, diode and current setting resistor. A high beta PNP transistor provides the current drive for all the segments. A reference voltage V3 is developed which compensates for variations in MOS process parameters and the variations in the voltage drop across the LED. The resistor sets the current in the reference LED which sets the reference voltage V3 which in turn sets the current in the LEDs equal to resistor current minus the base current of the transistor. Variation in second supply voltage does not vary the LED currents so long as the PNP transistor is kept operating in the linear mode. Full wave rectified power supply without any filtering can be used as a second supply voltage V2. The LED brightness can be varied by using a variable resistor.

Figure 6 shows a LED drive circuit which uses a single resistor. The resistor controls the total current flowing through all the segments. Brightness shall vary depending on number of segments that are "ON" at that time.

Radio Frequency Interference: All display outputs include circuitry to slow up the switching transition time to minimize radio frequency interference.

Clock Set Up Procedure: (MM5382)

1. Connect 110V supply.
2. Blinking 'OFF' displayed.
3. Momentarily connect alarm display set/snooze pin (13) to V_{DD} which removes "OFF" and displays first the alarm for 1.5 to 2 seconds, then real time.
4. Momentarily connect alarm "ON/OFF" to V_{SS}.
5. *Wait till the colon starts blinking.* (Approximately 2 seconds.)
6. Time setting
   a. Momentarily connect sequence pin (14) to V_{DD} display shows hour and AM or PM. Connect advance pin (11) to V_{DD} to advance hour.
   b. Connect pin (14) momentarily to V_{DD} display shows minutes, connect pin (11) to V_{DD} and set minutes.
   c. Connect pin (14) momentarily to V_{DD} display shows month, connect pin (11) to V_{DD} and set month.
   d. Connect pin (14) momentarily to V_{DD} display shows date, connect pin (11) to V_{DD} and set date.
   e. Connect pin (14) momentarily to V_{DD} and the real time is displayed at 2 Hz rate.
   f. Connect pin (14) momentarily to V_{DD} again and real time is displayed continuously.
7. Alarm setting
   a. Connect alarm display pin (13) to V_{DD} and hold it for more than 2 seconds. Alarm minutes will advance at slow rate.
   b. Connecting pin (11) and pin (13) to V_{DD} simultaneously will advance the alarm time at a fast rate.
   c. Set the desired alarm time.
8. Sleep time setting
   a. Connect, sleep display, pin (14) to V_{SS} and hold it for more than 2 seconds. Sleep time will decrement at slow rate.
   b. Connecting pin (11) and pin (14) to V_{DD} simultaneously will decrement the sleep time at a fast rate.
   c. Set the desired sleep time.
9. Connect pin 12 to V_{DD} to activate alarm.

Note: Time and date setting must be done only in the real time display mode.

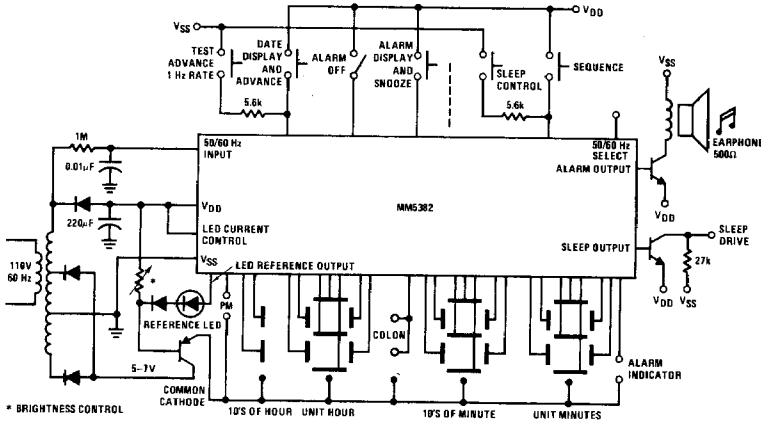


FIGURE 3. Calendar Alarm Clock Using the MM5382 and a LED Display

functional description (Continued)

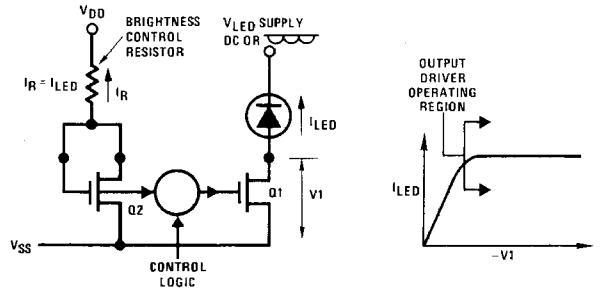


FIGURE 4(a). Low Current LED Drive Control Circuit (1–7 mA)

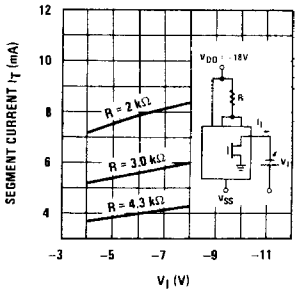


FIGURE 4(b). Segment Current vs V_I (V_{DD} at −18V) (Typical Output Characteristics)

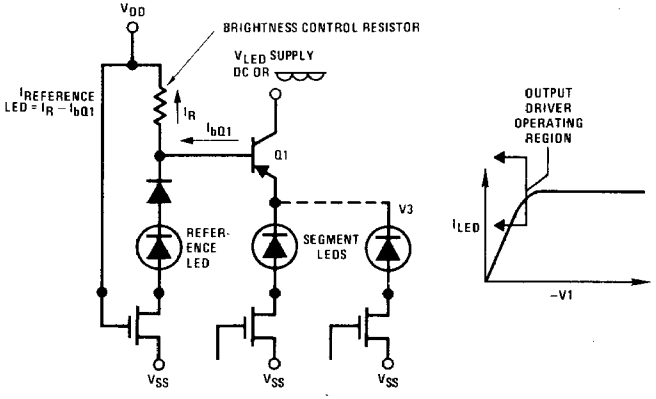


FIGURE 5(a). High Current LED Drive Current Circuits (7–15 mA)

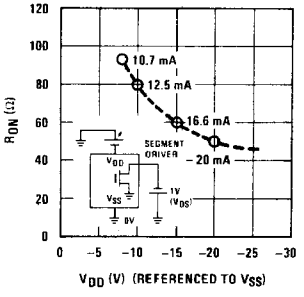


FIGURE 5(b). R_{ON} vs V_{DD} (V_{DS} at −1V) (Typical Output Characteristics)

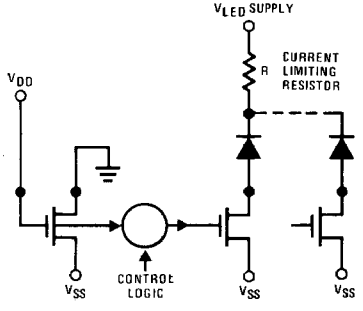


FIGURE 6. Simple LED Drive Circuit

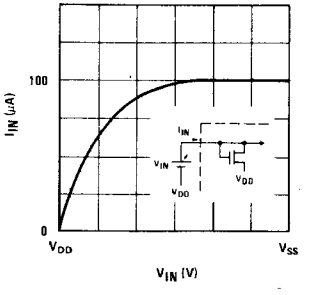


FIGURE 7. I_{IN} vs V_{IN} (Typical Input Depletion Load Characteristics)