GENLINX™ GS9000S
Serial Digital Decoder

DATA SHEET

GS9000S

NOT RECOMMENDED FOR NEW DESIGNS

FEATURES

- **fully compatible with SMPTE 259M**
- **decodes 8 and 10 bit serial digital signals for data rates to 300 Mb/s**
- **pin and function compatible with GS9000B and GS9000**
- **250 mW power dissipation at 270 MHz clock rates**
- **incorporates an automatic standards selection function with the GS9005A Receiver or GS9015A Reclocker**
- **operates from single +5 or -5 volt supply**
- **enables an adjustment-free Deserializer system when used with GS9010A and GS9005A or GS9015A**
- **28 pin PLCC packaging**

APPLICATIONS

- $4f_{SC}$ and 270 Mb/s , 4:2:2 serial digital interfaces
- Automatic standards select controller for serial routing and distribution applications using GS9005A Receiver or GS9015A Reclocker

DEVICE DESCRIPTION

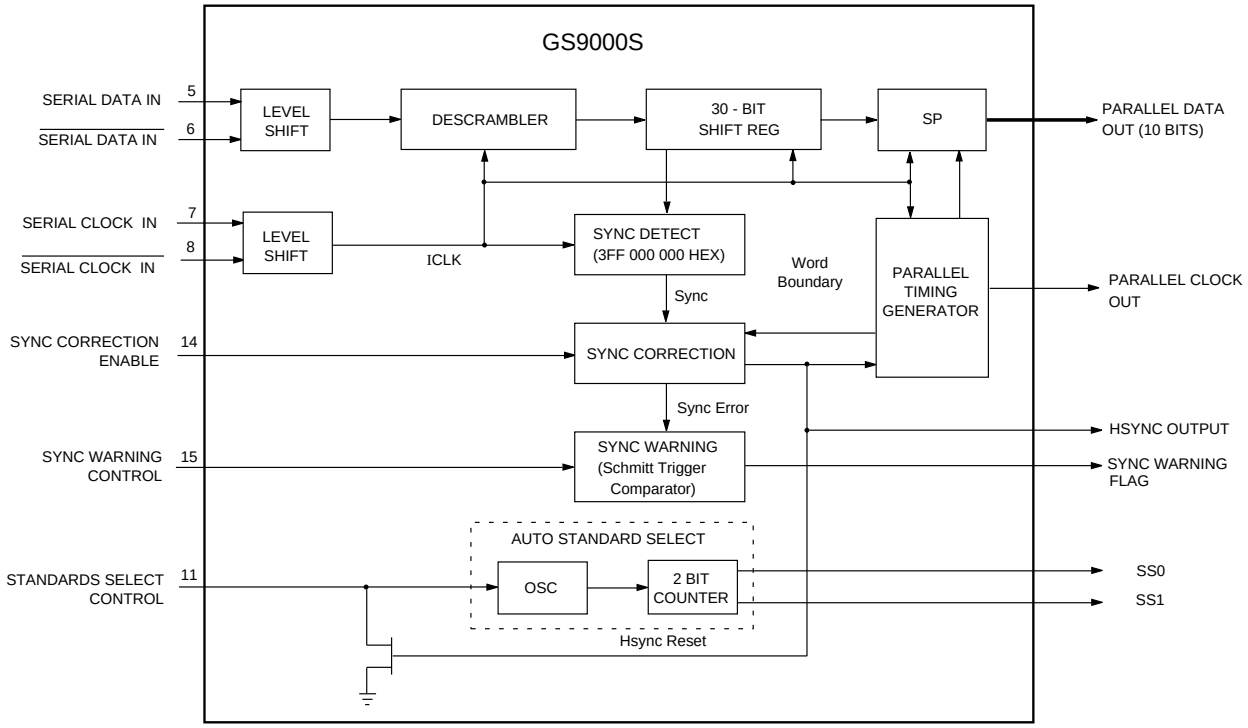
The GS9000S is a CMOS integrated circuit specifically designed to deserialize SMPTE 259M serial digital signals at data rates to 300Mbps.

The device incorporates a descrambler, serial to parallel convertor, sync processing unit, sync warning unit and automatic standards select circuitry.

Differential pseudo-ECL inputs for both serial clock and data are internally level shifted to CMOS levels. Digital outputs such as parallel data, parallel clock, HSYNC, Sync Warning and Standard Select are all TTL compatible.

The GS9000S is designed to directly interface with the GS9005A Reclocking Receiver to form a complete SMPTE-serial-in to CMOS level parallel-out deserializer. The GS9000S may also be used with the GS9010A and the GS9005A to form an adjustment-free receiving system which automatically adapts to all serial digital data rates. The GS9015A can replace the GS9005A in GS9000S applications where cable equalization is not required.

The GS9000S is packaged in a 28 pin PLCC and operates from a single 5 volt, ±5% power supply.



FUNCTIONAL BLOCK DIAGRAM

Revision Date: December 1999

Document No. 521 - 80 - 02

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GS9000S DECODER - DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	Operating Range	4.75	5.00	5.25	V	
Power Consumption	P_C	f = 270 MHz (see Fig. 8)	-	250	-	mW	
Input Resistance	R_{IN}		-	10	-	MΩ	
Input Capacitance	C_{IN}		-	5	10	pF	
CMOS Input Voltage	VIH_{MIN}	T_A = 25°C	3.4	-	-	V	
	VIL_{MAX}		-	-	1.5	V	
Output Voltage	VOH_{MIN}	T_A = 25°C	2.4	4.5	-	V	
	VOL_{MAX}	IOH = 4 mA	-	0.2	0.5	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}	-	-	±10	µA	
Serial Clock & Data Inputs							
Signal Swing	V_{IN}		700	800	1000	mV p-p	
Signal Offset	V_{INOS}		3.0	-	4.2	V	centre of swing

GS9000S DECODER - AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Serial Input Clock Frequency	f_{SCI}		100		300	MHz	
Serial Input Data Rate	DR_{SDI}		100		300	Mb/s	
Serial Data & Clock Inputs:		T_A = 25°C					
Risetime	t_R	T_{CLKL}	-	-	1.0	ns	
Setup	t_{SU}		1.0	-	-	ns	
Hold	t_{HOLD}		1.0	-	-	ns	
Parallel Clock: Jitter	t_{JCLK}	T_A = 25°C	-	1.0	-	ns p-p	
Parallel Data: Risetime	t_{R-PDn}	T_A = 25°C, C_L = 10pF	-	1.0	-	ns	20% to 80%
PDn to PCLK delay tolerance	t_D		-	-	±3	ns	rising edge of PCLK to bit period centre

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS9000SCPJ	28 Pin PLCC	0°C to 70°C
GS9000SCTJ	28 Pin PLCC Tape	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage (V_S=V_{DD}-V_{SS})	7 V
Input Voltage Range (any input)	-0.3 to (V_{DD}+0.3) V
DC Input Current (any one input)25 mW	±10 µA
Power Dissipation	400 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	260°C

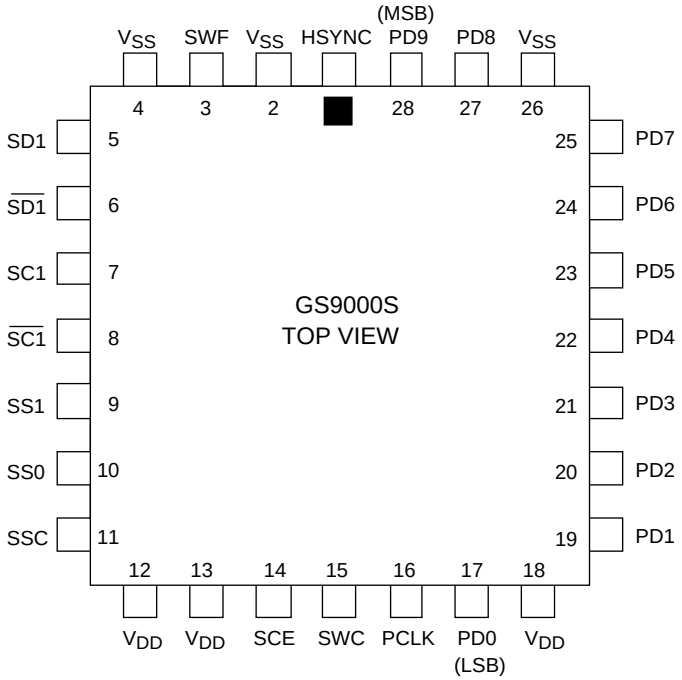


Fig. 1 GS9000S Pin Outs, 28 Pin PLCC Package

GS9000S PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	HSYNC	Output	Horizontal Sync Output. CMOS (TTL compatible) output that toggles for each TRS detected.
2	V_{SS}		Power Supply. Most negative power supply connection.
3	SWF	Output	Sync Error Warning Flag. CMOS (TTL compatible) active high output that indicates the preselected HSYNC Error Rate (HER). The HER is set with an RC time constant on the SWC input.
4	V_{SS}		Power Supply. Most negative power supply connection.
5,6	SDI/$\overline{\text{SDI}}$	Inputs	Differential, pseudo-ECL serial data inputs. ECL voltage levels with offset of 3V to 4.2V for operation up to 300 MHz. See AC characteristics for details.
7,8	SCI/$\overline{\text{SCI}}$	Inputs	Differential, pseudo-ECL serial clock inputs. ECL voltage levels with offset of 3V to 4.2V for operation up to 300 MHz. See AC characteristics for details.
9,10	SS1/SS0	Output	Standard Select Outputs. CMOS (TTL compatible) outputs used with the GS9005A Receiver in order to perform an automatic standards select function. These outputs are generated by a 2 bit internal binary counter which stops cycling when there is no CARRIER present at the GS9005A Receiver input or when a valid TRS is detected by the GS9000S.
11	SSC	Input	Standards Select Control. Analog input used to set a time constant for the standards select hunt period. An external RC sets the time constant. When a GS9005A Receiver is used, the open collector CARRIER DETECT output also connects to this pin in order to enable or disable the internal 2 bit binary counter which controls the hunting process.
12	V_{DD}		Power Supply. Most positive power supply connection.
13	V_{DD}		Power Supply. Most positive power supply connection.
14	SCE	Input	Sync Correction Enable. Active high CMOS input which enables sync correction by not resetting the GS9000S's internal parallel timing on the first sync error. If the next incoming sync is in error, internal parallel timing will be reset. This is to guard against spurious HSYNC errors. When SCE is low, a valid sync will always reset the GS9000S's parallel timing generator.

GS9000S PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
15	SWC	Input	Sync Warning Control. Analog input used to set the HSYNC Error Rate (HER). This is accomplished by an external RC time constant connected to this pin.
16	PCLK	Output	Parallel Clock Output. CMOS (TTL compatible) clock output where the rising edge of the clock is located at the centre of the parallel data window within a given tolerance. See Fig. 2.
17	PD0	Output	Parallel Data Output - Bit 0 (LSB). CMOS (TTL compatible) descrambled parallel data output from the serial to parallel convertor representing the least significant bit (LSB).
18	V_{DD}		Power Supply. Most positive power supply connection.
19 - 25	PD1 - PD7	Outputs	Parallel Data Outputs - Bit 1 to Bit 7. CMOS (TTL compatible) descrambled parallel data outputs from the serial to parallel convertor representing data bit 1 through data bit 7.
26	V_{SS}		Power Supply. Most negative power supply connection.
27	PD8	Output	Parallel Data Output. CMOS (TTL compatible) descrambled parallel data output from the serial to parallel convertor representing data bit 8.
28	PD9	Output	Parallel Data Output - Bit 9 (MSB). CMOS (TTL compatible) descrambled data output from the serial to parallel convertor representing the most significant bit (MSB).

INPUT / OUTPUT CIRCUITS

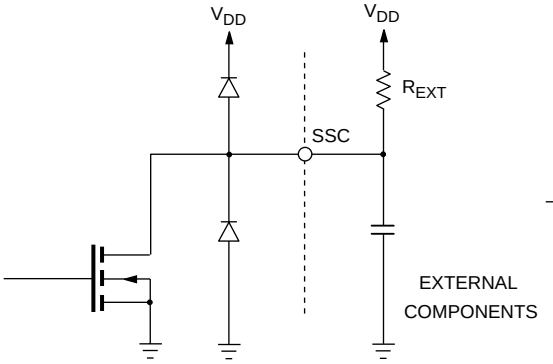


Fig. 2 Pin 11 SSC

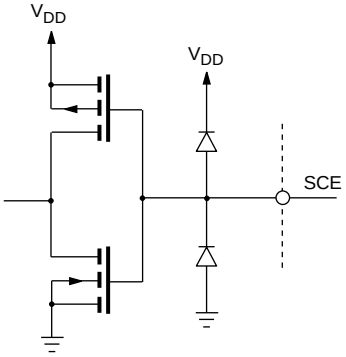


Fig. 3 Pin 14 SCE

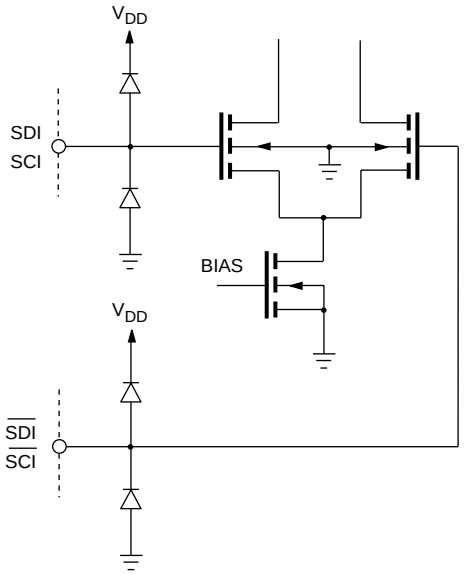


Fig. 4 Pins 5 - 8 SDI - SCI

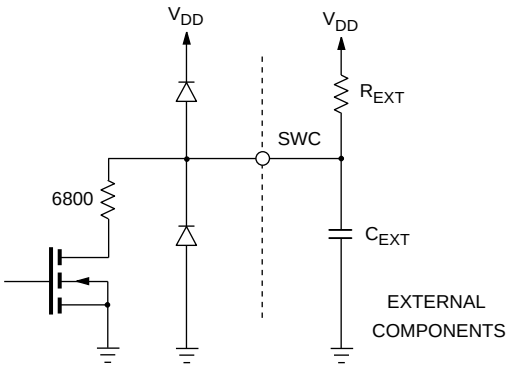


Fig. 5 Pin 15 SWC

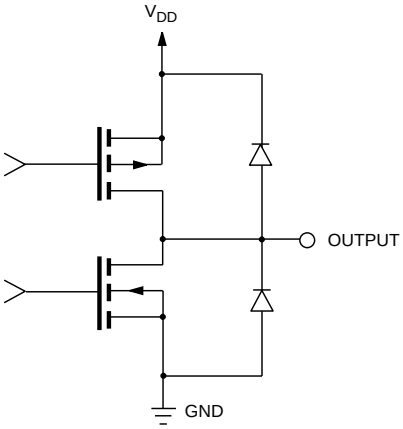


Fig. 6 Pins 3, 16, 17, 19 - 25, 27, 28
SWF, HSYNC, SSI, SSD, PCLK, PD0-9

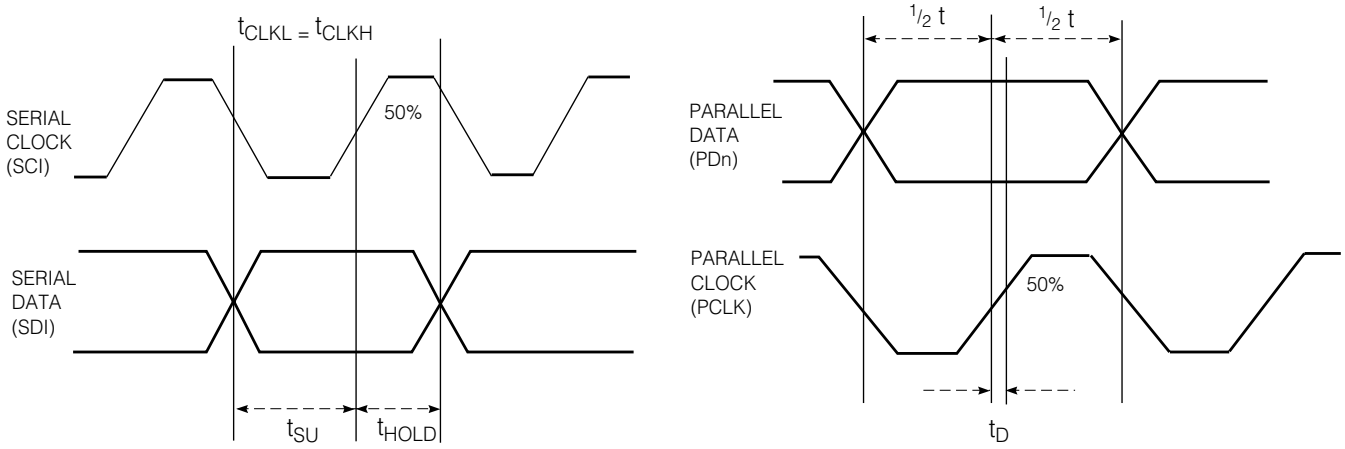


Fig. 7 Waveforms

TEST SET-UP & APPLICATION INFORMATION

Figure 9 shows the test set-up for the GS9000S operating from a V_{DD} supply of +5 volts. The differential pseudo ECL inputs for DATA and CLOCK (pins 5,6,7 and 8) must be biased between +3 and +4.2 volts. In the circuit shown, these inputs with the resistor values shown, can be directly driven from the outputs of the GS9005A Reclocking Receiver.

In other cases, such as true ECL level driver outputs, two biasing resistors are needed on the DATA and CLOCK inputs and the signals must be AC coupled.

It is critical that the decoupling capacitors connected to pins 12,13 and 18 be chip types and be located as close as possible to the device pins.

In order to maintain very short interconnections when interfacing with the GS9005A Receiver, the critical high speed inputs such as Serial Data (pins 5 and 6) and Serial Clock (pins 7 and 8) are located along one side of the device package.

If the automatic standard select function is not used, the Standard Select bits (pins 9 and 10) do not need to be connected, however the control input (pin 11) should be grounded.

TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25° C unless otherwise shown)

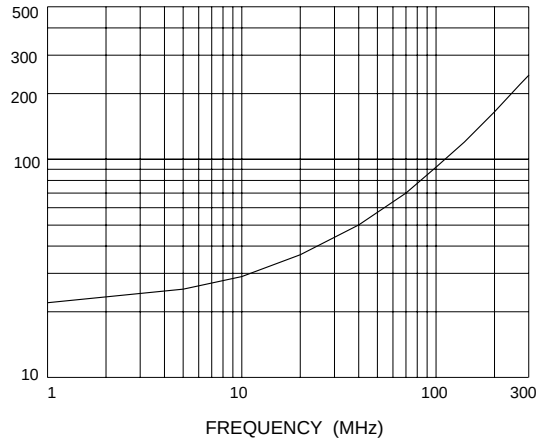


Fig. 8 Power Consumption

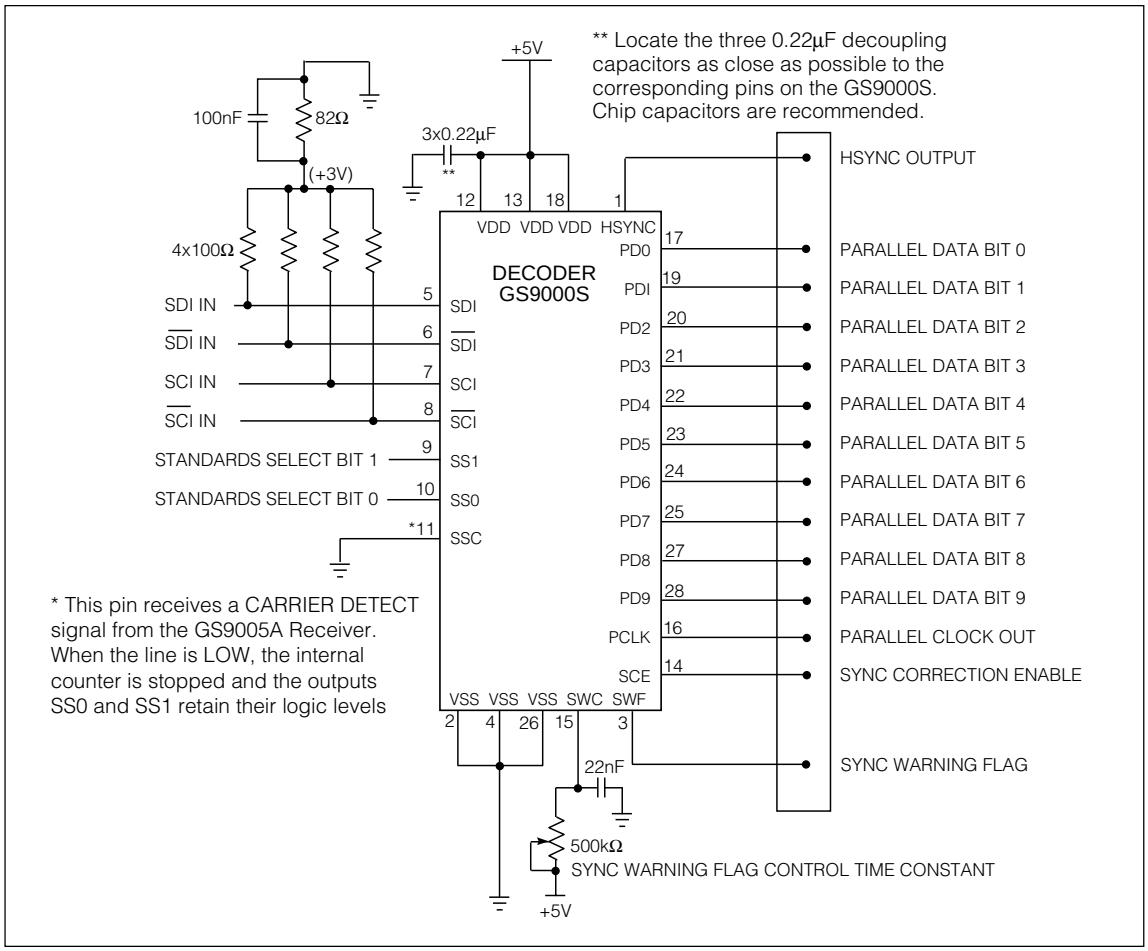
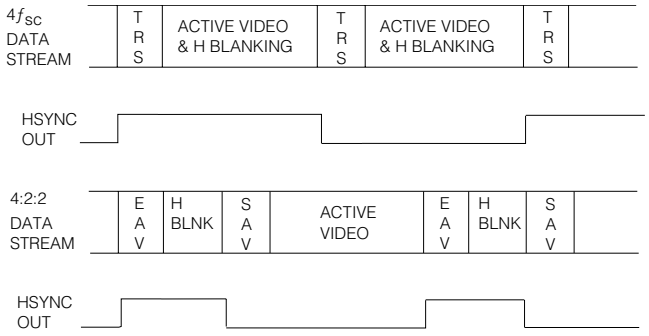


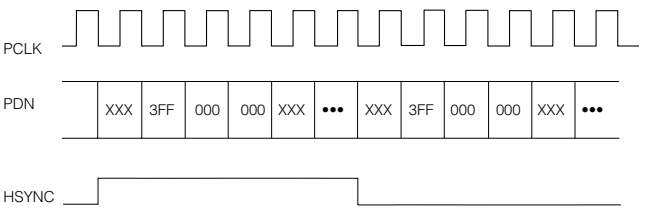
Fig. 9 GS9000S Test Set-Up

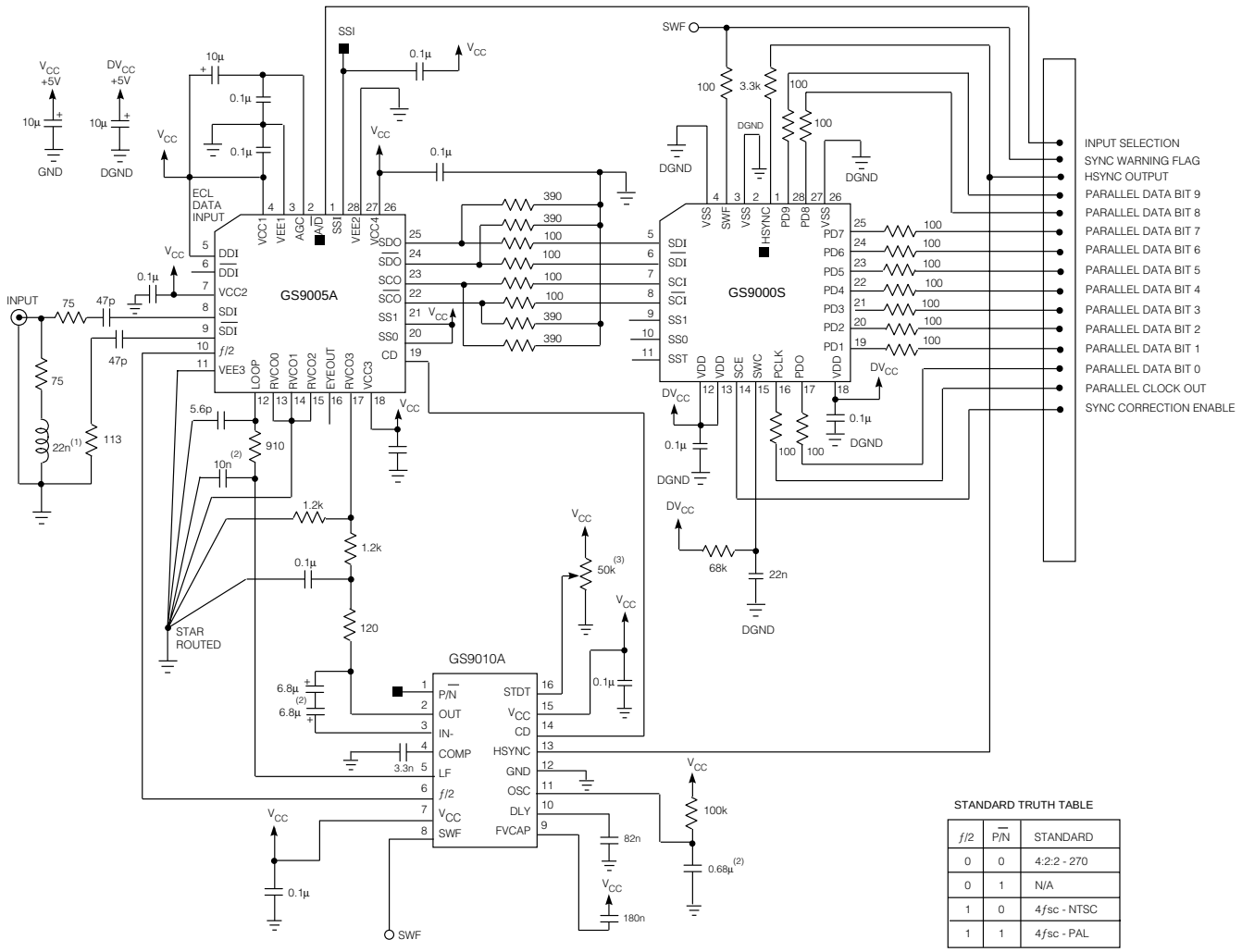
With correctly synchronized serial data and clock connected to the GS9000S, the HSYNC output (pin 1) will toggle for each HSYNC detected. The Parallel Data bits PD0 through PD9 along with the Parallel Clock can be observed on an oscilloscope or fed to a logic analyzer. These outputs can also be fed through a suitable TTL to ECL converter to directly drive parallel inputs to receiving equipment such as monitors or digital to analog converters.

In operation, the HSYNC output from the GS9000S decoder toggles on each occurrence of the timing reference signal (TRS). The state of the HSYNC output is not significant, just the time at which it toggles.



The HSYNC output toggles to indicate the presence of the TRS on the falling edge of PCLK, one data symbol prior to the output of the first word in the TRS. In the following diagram, data is indicated in 10 bit Hex.





STANDARD TRUTH TABLE

f/2	P/N	STANDARD
0	0	4:2:2 - 270
0	1	N/A
1	0	4fsc - NTSC
1	1	4fsc - PAL

(1) Typical value for input return loss matching

(2) To reduce board space, the two anti-series 6.8µF capacitors (connected across pins 2 and 3 of the GS9010A) may be replaced with a 1.0 µF non-polarized capacitor provided that:

(a) the 0.68 µF capacitor connected to the OSC pin (11) of the GS9010A is replaced with a 0.33 µF capacitor and

(b) the GS9005A /15A Loop Filter Capacitor is 10nF.

(3) Remove this potentiometer if P/N function is not required, and ground pin 16 of the GS9010A.

Fig. 10 Application Circuit - Adjustment Free Multistandard Serial to Parallel Convertor

GS9000S, GS9005A and GS9010A INTERCONNECTIONS

Figure 10 shows an application of the GS9000S in an adjustment free, multi-standard serial to parallel convertor. This circuit uses the GS9010A Automatic Tuning Sub-system IC and a GS9005A Serial Digital Receiver. The GS9005A may be replaced with a GS9015A Reclocker IC if cable equalization is not required.

The GS9010A ATS eliminates the need to manually set or externally temperature compensate the Receiver or Reclocker VCO. The GS9010A can also determine whether the incoming data stream is 4*f*sc NTSC, 4*f*sc PAL or component 4:2:2.

The GS9010A includes a ramp generator/oscillator which repeatedly sweeps the Receiver/Reclocker VCO frequency over a set range until the system is correctly locked. An automatic fine tuning (AFT) loop maintains the VCO control voltage at it's centre point through continuous, long term adjustments of the VCO centre frequency.

During normal operation, the GS9000S Decoder provides continuous HSYNC pulses which disable the ramp/oscillator of the GS9010A. This maintains the correct Receiver/ Reclocker VCO frequency. When an interruption to the incoming data stream is detected by the Receiver/Reclocker, the Carrier Detect goes LOW and tri-states the AFT loop in order to maintain the correct VCO frequency for a period of about 2 seconds. This allows the Receiver/Reclocker to rapidly relock when the signal is re-established.

SYNC WARNING FLAG OPERATION

Each time HSYNC is not correctly detected, the Sync Warning Flag output (pin 3) will go HIGH. The RC network connected to the Sync Warning Control input (pin 15) sets the number of sync errors that will cause the SWF pin to go HIGH. The component values of the RC network shown in Figure 10 set the SWF error rate to approximately one HSYNC error in 10 lines. These component values are chosen for optimum performance of the SWF pin, and should not be adjusted.

Typically, HSYNC errors will become visible on a monitor before the SWF will provide an indication of HSYNC errors. As a result, the SWF function can be used in applications where the detection of significant signal degradation is desired.

A high SWF will go low as soon as the input error rate decreases below the set rate. This response time is determined by C, as mentioned earlier. A small amount of hysterisis in the comparator ensures noise immunity.

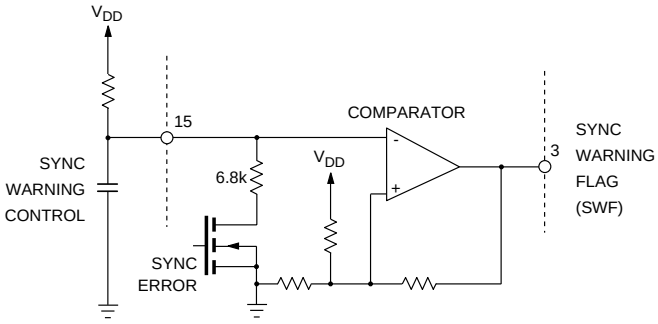


Fig. 11 Sync Warning Flag Circuit

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