Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

“Standard”:	Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
“High Quality”:	Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
“Specific”:	Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

APPLICATION OF N-ch POWER MOS FET 2SK278 TO 200 kHz SWITCHING REGULATOR

1. INTRODUCTION

The switching regulators are miniaturized very rapidly in order to satisfy the increasingly rigid requirements of equipment designers. Technical improvements on their elements and applications are introduced so quickly one after another.

The most significant trend of all is that the operating frequency of typical switching regulators has been successively raised from the previous level of 20 kHz to 50 kHz or even 100 kHz today. This realizes corresponding improvements of frequency characteristics of various devices and their applicability in elevated frequency environments.

It is against such background that Nippon Electric Company (NEC) is proud to offer on production basis N-ch power MOS FET 2SK278, a switching device designed to be compatible with 200 kHz which is the operating frequency level any next-generation switching regulators will naturally be required to attain.

In order to show an example of promising application potentials of 2SK278, this brochure describes a 200 kHz, 5 V, 10 A output forward type switching regulator where 2SK278 is used as the main switching device in combination with other elements capable of operating in 200 kHz environments.

2. GENERAL DESCRIPTION OF 2SK278

The absolute maximum ratings, electrical characteristics and external dimensions of 2SK278 are shown in Tables 1 and 2 and Fig. 1 respectively.

Table 1. Absolute Maximum Ratings (Ta = 25 °C)

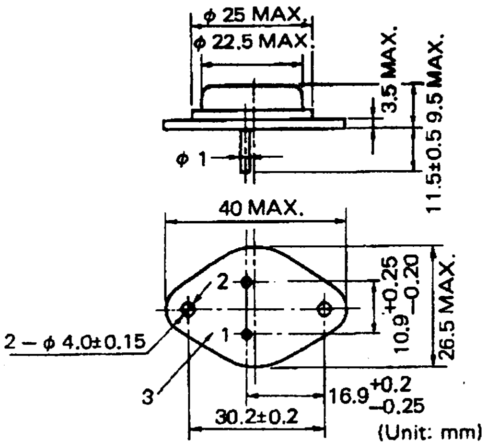
ITEM	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	$V_{GS} = 0$	400	V
Gate to Source Voltage	V_{GSS}	$V_{DS} = 0$	±20	V
Continuous Drain Current	$I_{D(DC)}$		7.0	A
Peak Drain Current	$I_{D(pulse)}$	PW ≦ 10 ms duty cycle ≦ 50 %	10	A
Total Power Dissipation	P_T	$T_C = 25$ °C	100	W
Maximum Channel Temperature	T_{ch}		150	°C
Storage Temperature	T_{stg}		−65~+150	°C

APPLICATION NOTE

APPLICATION OF N-ch POWER MOS FET 2SK278 TO 200 kHz SWITCHING REGULATOR

TEA—1023 MAR.—81

Nippon Electric Co.,Ltd.



1. Gate
2. Source
3. Drain

EIAJ : TC-3, TB-3
JEDEC : TO-3
IEC : C14A, B18

Schemetic Diagram

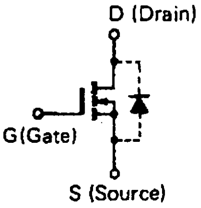


Fig.1 2SK278 Package Dimensions

Table 2. Electrical Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source Breakdown Voltage	BV_{DSS}	400			V	$V_{GS} = 0$ $I_D = 10$ mA
Gate Cutoff Current	I_{GSS}			±100	nA	$V_{DS} = 0$, $V_{GS} = \pm 20$ V
Drain Cutoff Current	I_{DSS}			10	mA	$V_{DS} = 400$ V, $V_{GS} = 0$
Gate to Source Cutoff Voltage	$V_{GS\ (off)}$	0.4	1	3	V	$V_{DS} = 10$ V, $I_D = 50$ mA
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	0.6	1.0		S	$V_{DS} = 10$ V, $I_D = 3$ A
Drain to Source On Resistance	$R_{DS\ (ON)}$		1.0	1.5	Ω	$V_{GS} = 15$ V, $I_D = 4$ A
Input Capacitance	C_{iss}		950	1500	pF	$V_{DS} = 10$ V, $V_{GS} = -5$ V, f = 1 MHz
Output Capacitance	C_{oss}		600		pF	
Reverse Transfer Capacitance	C_{rss}		10		pF	
Turn-on Delay Time	$t_{d\ (on)}$		20	50	ns	$I_D = 2$ A, $V_{GS(on)} = 10$ V, $V_{GS(off)} = 0$, $R_L = 75\ \Omega$, $V_{CC} \fallingdotseq 150$ V, PW = 1 μs, duty cycle ≦ 1 %
Rise Time	t_r		20	50	ns	
Turn-off Delay Time	$t_{d\ (off)}$		25	50	ns	
Fall Time	t_f		35	50	ns	

2SK278 is an N-channel MOS FET of vertical configuration, using the case as the drain. As it is also an enhancement type MOS FET, it is used in the same bias condition as the conventional bipolar NPN transistors as long as due attention is paid to the fact that its gate is voltagedriven.

In addition its V_{DSS} is rated at 400 V and its on-state resistance ($R_{DS(on)}$) is relatively small as the MOS FETs go while it attains a very high switching speed. These distinctive features join to justify the use of 2SK278 as an AC 100 V line operating type switching regulator in the frequency range of more than 100 kHz where the conventional bipolar transistors fail to respond quickly enough.

The structure of 2SK278 and external appearance of its element are shown in Figs. 2 and 3 respectively.

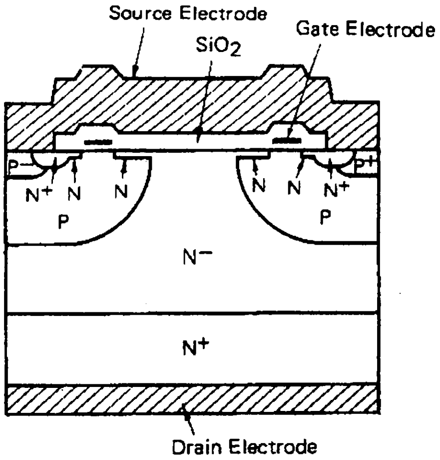


Fig.2 2SK278 Structure

Equivalent circuit of this device (see below) can be described as a cascading connection of three FETs. Junction FETs FET-3 and FET-2 have high breakdown voltage, and protect MOS FET stage FET-3 from high voltage exposure.

By this fact, 2SK278 can have high Drain to source breakdown voltage.

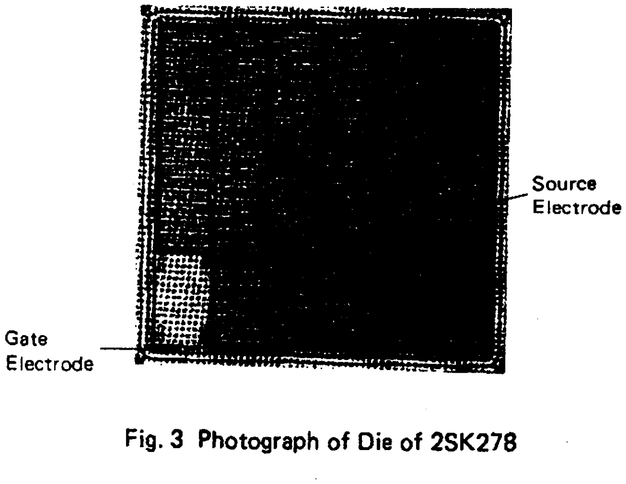
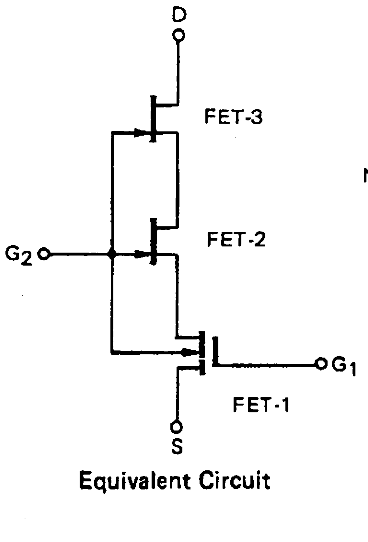


Fig. 3 Photograph of Die of 2SK278



Equivalent Circuit

Note:

G_1 : Gate Electrode of FET-1

G_2 : Gate Part of Equivalent Junction FETs FET-2 and FET-3

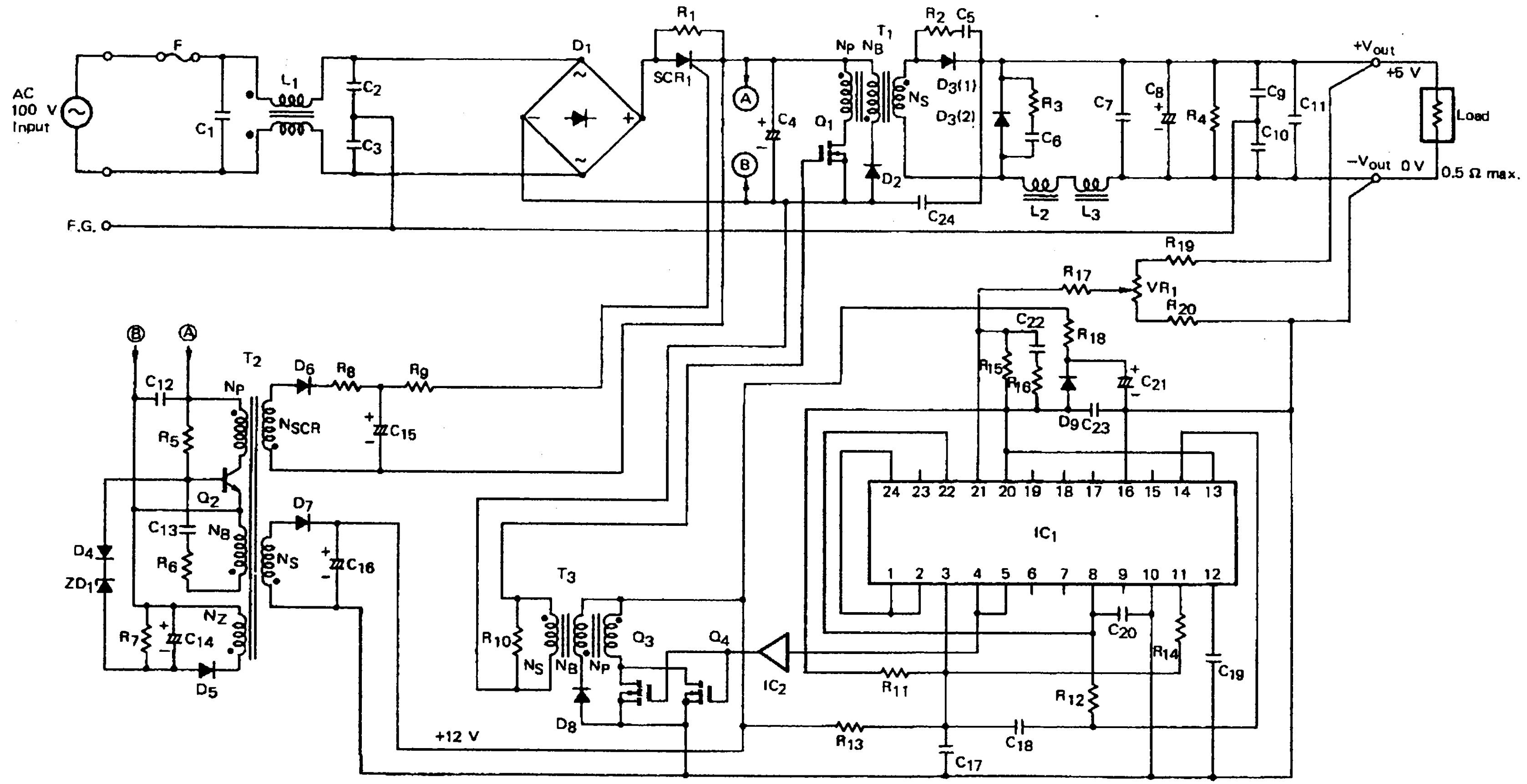


Fig.4 200 kHz Forward Type Switching Regulator Circuit

Table 3. Parts List

SYMBOL	NAME	RATINGS
C_1~C_3	Film Capacitors	0.22 μF, 500 V
C_4	Al electrolythic capa.	470 μF, 160 V
$C_{5,6}$	mylar film capa.	1000 pF, 50 V
C_7	film capa.	2.2 μF, 50 V
C_8	Al electrolythic capa.	4700 μF, 16 V
$C_{9,10}$	film capa.	0.22 μF, 500 V
C_{11}	mylar film capa.	0.47 μF, 50 V
C_{12}	film capa.	0.068 μF, 200 V
C_{13}	mylar film capa.	1500 pF, 50 V
C_{14}	Al electrolythic capa.	33 μF, 16 V
C_{15}	"	150 μF, 10 V
C_{16}	"	330 μF, 16 V
C_{17}	mylar film capa.	0.22 μF, 50 V
C_{18}	"	1500 pF, 50 V
C_{19}	ceramic capa.	470 pF, 50 V
C_{20}	mylar film capa.	0.22 μF, 50 V
C_{21}	Al electrolythic capa.	33 μF, 16 V
C_{22}	–	–
C_{23}	mylar film capa.	1000 pF, 50 V
C_{24}	film capa.	0.1 μF, 650 V
D_1	bridge rectifier	2B8M (400 V, 1.5 A) NEC
D_2	first recovery diode	F114D (400 V, 0.8 A) "
D_3	Schottky barrier diodes (common cathode)	20CSO4M (40 V, 20 A) "
D_4~D_6	diodes	1S953 "
$D_{7,8}$	"	1S954 "
D_9	diode	1S953 "
F	fuse	3 A
IC_1	Sw. Reg. Controller	ZN1066E Ferranti
IC_2	LSTTL (Inverter)	μPB74LS00 NEC
L_1	Common mode choke coil for line filter	core: T12-125 (dastcore) N_1=N_2=10Turns D=0.6 mm φ 2 parallel
L_2	choke coilfor smoothing circuit	core: EI-22H_7c_1 TDK N=6Turns D=0.6 mm φ 2 parallel 3 layer L=50 μH
L_3	choke coil for smoothing circuit	core: T8-125 N=8Turns D=0.7 mm φ 4 parallel L=4.6 μH
Q_1	Power MOS FET	2SK278 (400 V, 7 A) NEC
Q_2	V MOS FET	2SC2752 400 V, 2 A TO-126 NEC
Q_3, Q_4		VN66AF (60 V, 2 A) Siliconix
R_1	cement resistor	15 Ω, 5 W
$R_{2,3}$	carbon film resistor	4.7 Ω, 1/2 W
R_4	solid resistor	50 Ω, 1 W
R_5	carbon film resistor	150 kΩ
R_6	"	100 Ω
R_7	"	4.7 kΩ
R_8	"	220 Ω
R_9	"	100 Ω
R_{10}	"	240 Ω, 1/2 W
$R_{11,17}$	"	10 kΩ
R_{12}	"	4.7 kΩ
R_{13}	"	150 Ω, 1/2 W
R_{14}	metal film resistor	6.9 kΩ
R_{15}	carbon film resistor	1.5 MΩ
R_{16}	"	–
R_{18}	"	6.8 kΩ
$R_{19,20}$	metal film resistor	1 kΩ
SCR_1	SCR	5P2M (5 A, 200 V) NEC
T_1	Output transformer	core: PQ20/20H7C1 TDK Np=27Turns, Dp=0.4 mm φ 3 layers Ns=4 Turns, Ds=0.4 mm φ 6 parallel 3 layers NB=27Turns, DB=0.4 mm φ 1 layers
T_2	transformer for auxiliary power supply	core: EP-13H_7c_1 TDK Np=95Turns, Dp=0.2 mm φ Lp=1.75 mH NB=4Turns, DB=0.25 mm φ Ns=14Turns, Ds=0.25 mm φ 2 parallel 2 layers Nz=14Turns, Dz=0.25 mm φ N_{SCR}=4Turns, D_{SCR}=0.25 mm φ
T_3	pulse transformer for gate driving	core: EP-10H_{5A} TDK Np=Ns=N_B=18 Turns Dp=Ds=D_B=0.25 mm φ Lp=92 μH
VR_1	Variable resistor	PN822H102H (NEOPOT) NEC
ZD_1	Zenner diode	RD13EB (13 V, 400 mW) NEC

3. APPLICATION TO 200 kHz SWITCHING REGULATOR

A trial model of the 5 V, 10 A output forward type switching regulator where 2SK278 is used in the output stage, is described in the following pages.

3.1 Specifications of Power Supply

Input voltage : AC 100 V ± 15 % (50 or 60 Hz)
Output voltage, current: DC 5 V ± 5 %, 10 A max.
Operating frequency : f = 200 kHz

3.2 Design Key Points

As the trial model switching regulator must operate at a definitely high frequency than conventional switching regulators, it is necessary to introduce many improvements in terms of transformer design, etc. The more important of them incorporated in the trial model switching regulator are listed in Table 4.

Table 4. 200 kHz Switching Regular Design Key Points

ITEM	IMPROVEMENT POLICY	CONCRETE MEASURE TAKEN
Prevention of rush current into line	Adoption of slow start circuit	SCR installed in parallel to limiting resistor on line side
Miniaturization of auxiliary power supply	Adoption of DC-DC convertor	Adoption of fly-back type DC-DC convertor (simple switching regulat circuit added, f=150 kHz, Po=1.5W).
Prevention of rush current into invertor	Adoption of soft start circuit	Control IC amplifier output provided with time constant with addition of Capacitor and Resiste.
Reduced radiation noise of secondary rectifying diode	Fixed diode case potential	Secondary choke coil installed on GND line side so that diode case potential does not fluctuate..
Output transformer frequency band extension	Reduced primary to secondary leakage inductance	Improved coil winding.
Transient response/ regulation coexistence	Adoption of combined choke coil	Two choke coils serially connected, realizing two different L values by current value.

3.3 Circuit Designs

(1) Slow start circuit

As the primary smoothing circuit is designed to receive input from capacitor C_4, this slow start circuit is used to perform charging the capacitor gradually enough to prevent the occurrence of a rush current when the switch is turned on.

Concretely charging C_4 starts through R_1. As the auxiliary power supply circuit (DC-DC convertor) of Q_2, etc. is actuated, the N_{SCR} coil generates a voltage, which is used to charge C_{15} at a certain time constant through the time constant circuit composed of R_8 and C_{15}. The charged C_{15} trigers SCR_1 through R_9.

In this case the surge current to SCR_1 must be provided with a sufficiently large margin against the maximum rating of I_{TSM} = 80 A. (Usually below 20 A)

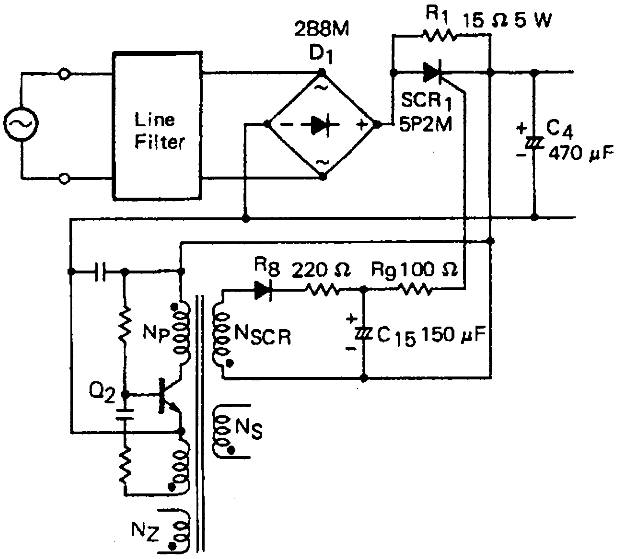


Fig.5 Slow Start Circuit

(2) Auxiliary power supply

Circuit diagram of auxiliary power supply DC-DC convertor is shown in Fig. 6. This convertor is of fly-back type, and operates as a simplified stabilizing circuit by providing the positive feedback from N_B to the base for self-excited oscillation and, at the same time, connecting output voltage of N_Z which has as many turns of winding as N_S, to the base of Q_2 through D_4 and ZD.

This convertor has NTC2752 as Q_2 and operates on the frequency of about 150 kHz. Its output profiles are roughly as follows.

For driver control IC bias : V_S = 14 V

For SCR_1 drive : V_{SCR} = 5 V

For stabilization (N_Z coil output): V_Z = 14 V

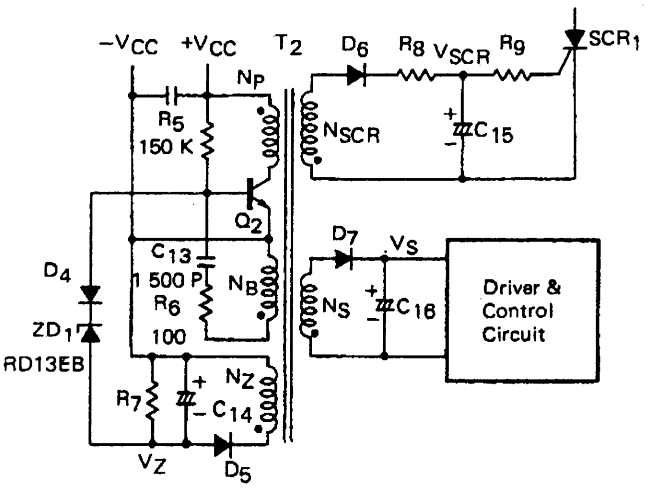


Fig.6 Auxiliary Power Supply Circuit

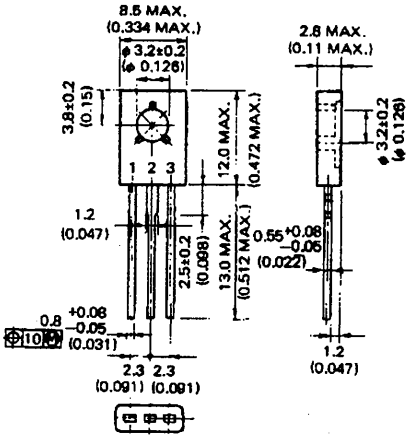
ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta=25 °C)			
Collector to Emitter Voltage	V_{CEO}	400	V
Emitter to Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	$I_{C(DC)}$	500	mA
Peak Collector Current	$I_{C(pulse)}$*	1000	mA
Continuous Base Current	$I_{B(DC)}$	250	mA
Maximum Power Dissipations			
Total Power Dissipation (Ta=25 °C)	P_T	1.0	W
Total Power Dissipation (T_C=25 °C)	P_T	20.8	W
Maximum Temperatures			
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Thermal Resistance			
Junction to Case	$R_{th(j\text{-}c)}$	6.0	°C/W

*Pulsed PW ≦ 300 µs, duty cycle ≦ 10 %

PACKAGE DIMENSIONS

in millimeters (inches)



1. Emitter (E)
2. Collector (C)
3. Base (B)
4. Fin (Collector)

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

Fig.7 Outlined Specifications of NTC2752

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	400			V	I_C=10 mA, I_B=0
Collector Cutoff Current	I_{CBO}			10	µA	V_{CB}=400 V, I_E=0
Emitter Cutoff Current	I_{EBO}			10	µA	V_{EB}=5.0 V, I_C=0
DC Current Gain	h_{FE1}	20		80		V_{CE}=5 V, I_C=50 mA*
	h_{FE2}	10				V_{CE}=5 V, I_C=0.3 A*
Collector Saturation Voltage	$V_{CE(sat)}$			1.0	V	I_C=300 mA, I_B=60 mA*
Base Saturation Voltage	$V_{BE(sat)}$			1.2	V	
Turn On Time	t_{on}		0.5	1.0	µs	I_C=0.3 A, I_{VL}=I_{B2}=60 mA, V_{CC}=150 V, R_L=500 Ω, PW=50 µs, duty cycle ≦ 2%
Storage Time	t_{stg}		2.3	2.5	µs	
Fall Time	t_f		0.35	1.0	µs	

* Pulsed PW ≦ 350 µs, duty cycle ≦ 2 %

Caution: This transistor NTC2752 is underdevelopment device, and was production of this transistor will be started middle of 1981.

(3) Control circuit

With the conventional operating frequency of less than 100 kHz the control circuits may be built around standard ICs. The operating frequency of 200 kHz means, however, a shortened cycle of 5µs. So, standard ICs are not fully acceptable in such operating environment because their input/output delay runs almost 500 ns due to tpd characteristics of their comparators, and because the amplifiers' frequency characteristics are limited in high frequency range terms.

(The 200 kHz operation must be provided with tpd ≦ 100 ns and the amplifier frequency characteristics of more than 200 kHz for A_V = 40 dB.)

As a result, ZN1066E of Ferranti Electric Inc., is used for the trial model switching regulator.

(The frequency characteristics of the amplifier built in this IC is about 3 MHz for A_V = 40 dB.)

This IC contains two of these amplifiers, each of which is provided with the common mode input voltage range of 1 V to 2.8 V and designed to operate on a single power supply, not accepting 0 V. As a result, no excess current protection circuit is provided.

(4) Main transformer T_1 design

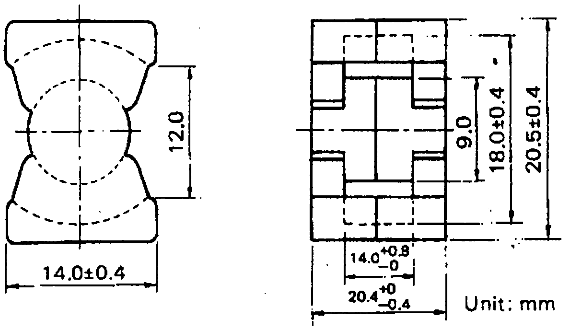
PQ core of TDK is adopted for main transformer T_1. The following TDK document was referenced in drawing up T_1 design. Interested readers are advised to consult it.

Document title: PQ CORES FOR SWITCHING POWER SUPRIIES No. 79L-2

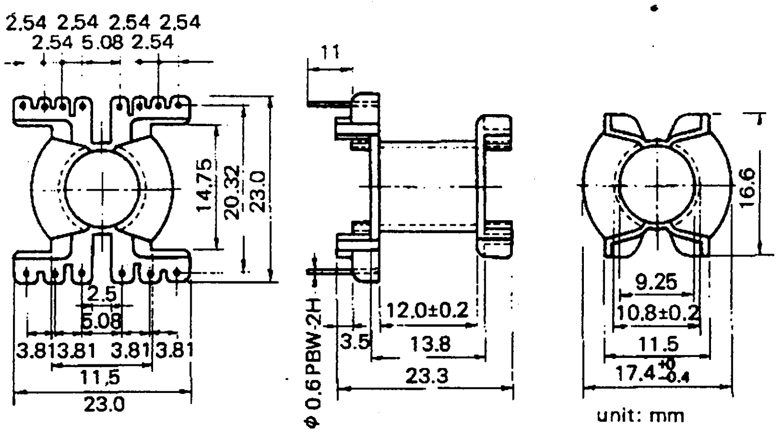
Core used: PQ 20/20 H_{7C1}

The core and core bobbin shapes and core constant of PQ 20/20 H_{7C1} are shown in Fig. 8.

PQ 20/20 Shape



PQ 20/20 Bobbin Shape



Parameter			
Core Constant	C_1	mm^{-1}	0.738
Effective Magnetic Path Length	ℓe	mm	45.4
Effective Cross Sectional Area	Ae	mm^2	62
Effective Volume	Ve	mm^3	2790
Central Leg Cross Sectional Area	Acp	mm^2	61
Minimum Area of Acp	Acp(min)	mm^2	58.1
Actual Window Area	Acw	mm^2	65.8
Weight		g	15

Name	AL-value (nH/N^2)
H_{7C1}PQ20/20 Z-12	≥4260
(50 kHz, 3T 100 °C)	

Fig.8 PQ20/20 Core, Core Bobbin Shapes and Core Constant

– Decision on Turns of Coil Winding –

Forward constant (K_{FC}) = 0.3 is assumed for 200 kHz operation. The minimum value (Vin (min)) of the smoothing input voltage is found as follows.

Taking Vin = 85 V (min) and input = 10 A and consulting the O.H. Shade chart or calculating from the amount of electric charge from the smoothing capacitor due to invertor action,

$$\text{Vin (min)} = 95\ \text{V}$$

Assuming core temperature increase T_{up} at 35 °C, permissible power loss P_m is,

$$P_m = 1\ \text{W}$$

From the relationships $P_m = P_{LF} + P_{CU}$ and $P_{LF} = P_{CF}$ (minimal loss condition),

$$P_{LF} = P_{CU} = 0.5\ \text{W}$$

therefore total loss P_L is found as follows by $P_L = P_{LF}/K_{FC}$ which expresses the relationship between iron loss P_{LF} and K_{FC} in the forward convertor circuit,

$$P_L = 1.67\ \text{W}$$

The relationship between flux density at operation and P_L is expressed as follows:

$$Bm^{2.4} = \frac{P_L}{(Kh + Ke \cdot f)\, f \cdot Ve}$$

therefore

$$Bm = \left\{ \frac{1.67}{(4.9 \cdot 10^{-17} + 1.7 \cdot 10^{-22} \cdot 200 \cdot 10^{3}) \cdot 200 \cdot 10^{3} \cdot 2310} \right\}^{\frac{1}{2.4}} \cdot 10^{-4}$$

$$= 0.1523\ [\text{T}]$$

As a result, from $\Delta B = 0.12$ T (25 °C) and $A_{CP} = 61\ \text{mm}^2$ N_P, the number of primary winding turns, is expressed as follows.

$$N_P = \frac{\text{Vin (min)} \cdot \tau_0 \max}{\Delta B \cdot A_{cp}}$$

Assuming τomax = 0.45T and T = 5 μs

$$N_P = \frac{95 \times 2.25 \times 10^{-6}}{0.12 \times 61 \times 10^{-6}} = 29.2 \fallingdotseq 30.\ [\text{Turns}]$$

– Decision on Secondary Winding –

$$N_S = \frac{N_P}{\text{Vin (min)}} \cdot V_S \text{ and } V_S = \frac{V_O + V_F + V_\ell}{D_{max}}$$

where V_ℓ = line drop voltage.

$$N_S = \frac{N_P\,(V_O + V_F + V_\ell)}{\text{Vin (min)} \cdot \text{Dmax}}$$

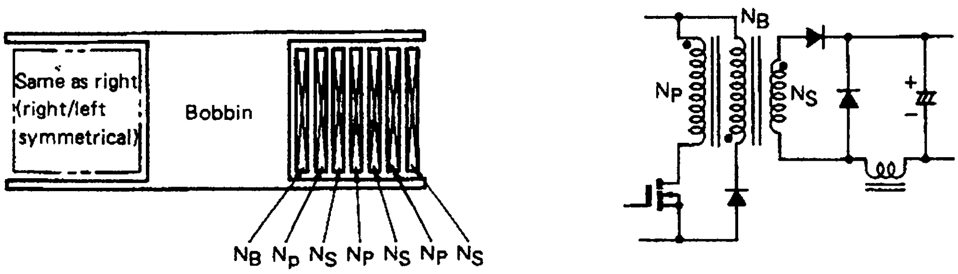
where $V_F = 0.6$ V, $V_O = 5$ V, $V_\ell = 0.2$ V and Dmax = 45 %.

Therefore

$$N_S = \frac{30 \times 5.8}{95 \times 0.45} = 4.07\ [\text{Turns}]$$

– Winding –

Avoiding the formation of any air gap toward the bobbin edges is especially important to minimize leakage inductance. The sandwich method of winding the primary and secondary coils is also preferred for the purpose. The winding configuration shown in Fig. 9 is adopted, reflecting the outcome of a series of trials and errors.



Np=27 Turns	NB=27 Turns	NS=4 Turns
Dp=0.4 mm φ	DB=0.4 mm φ	DS=0.4 mm φ 6 parallel
3 layers	1 layers	3 layers

Fig. 9

Note: Against the design target of $N_p = 30$ [ ] $N_p = 27$ [ ] was the actual limit attainable with the 0.4 mm ϕ wire. Therefore $N_p = 27$ [ ] is used with the trial model switching regulator.

As a result, the constants above assume the following values.

$$\text{From } \Phi = \frac{V_{in(min)} \cdot \tau_{omax}}{N_p} = 7.92 \text{ [wb]}$$

$\Delta B = 0.13$ T, $B_m = 0.16$ T, $P_L = 2.27$ W and $P_{LF} = 0.681$ W

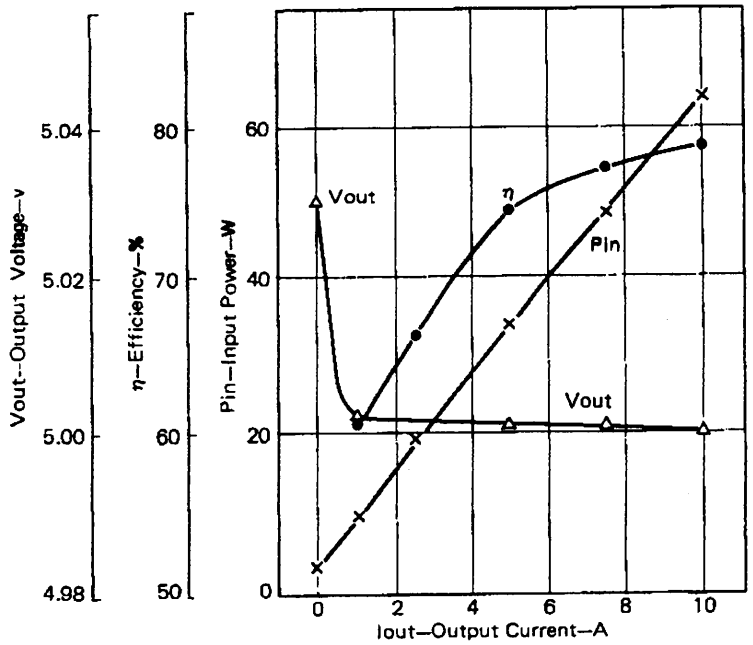
4. RESULTS

The switching regulator designed and manufactured as described in the following pages were tested and the results are shown in Table 5 and Fig. 10.

Table 5 Trial Model Switching Regulator Performance Evaluation Results

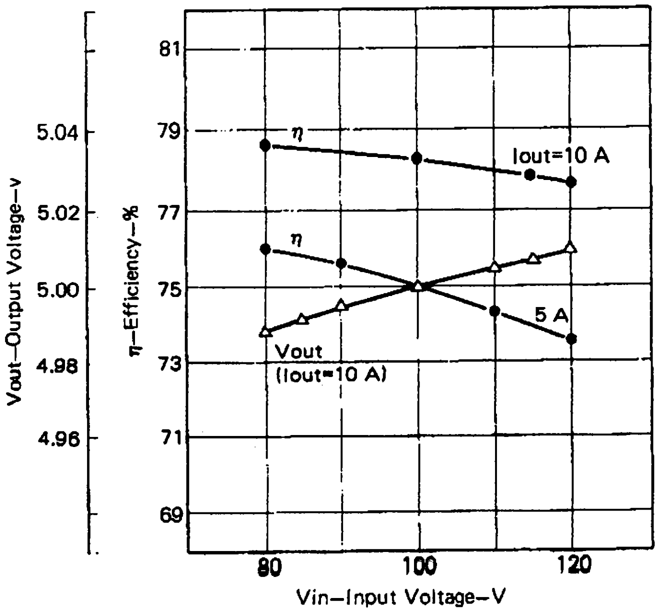
Table 5.

Item	Conditions	Measured value
Line Regulation (%) ΔV_{out} ($\Delta V_{out}/V_{out}$)	V_{in}=85~115 V V_{out}=5 V, I_{out}=10 A	16 mV(0.32 %)
Load Regulation (%) ΔV_{out} ($\Delta V_{out}/V_{out}$)	I_{out}=0~10 A (0 to rated load) V_{in}=100 V, V_{out}=5 V	30 mV(0.60 %)
Output ripple voltage Vripple	V_{in}=100 V V_{out}=5 V, I_{out}=10 A (excluding output noise, p–p value)	50 mVp–p
Efficiency η	V_{in}=100 V V_{out}=5 V, I_{out}=10 A	78.4%
External shape	Without casing	34(W) X 170(D) X 110(H) (unit: mm)



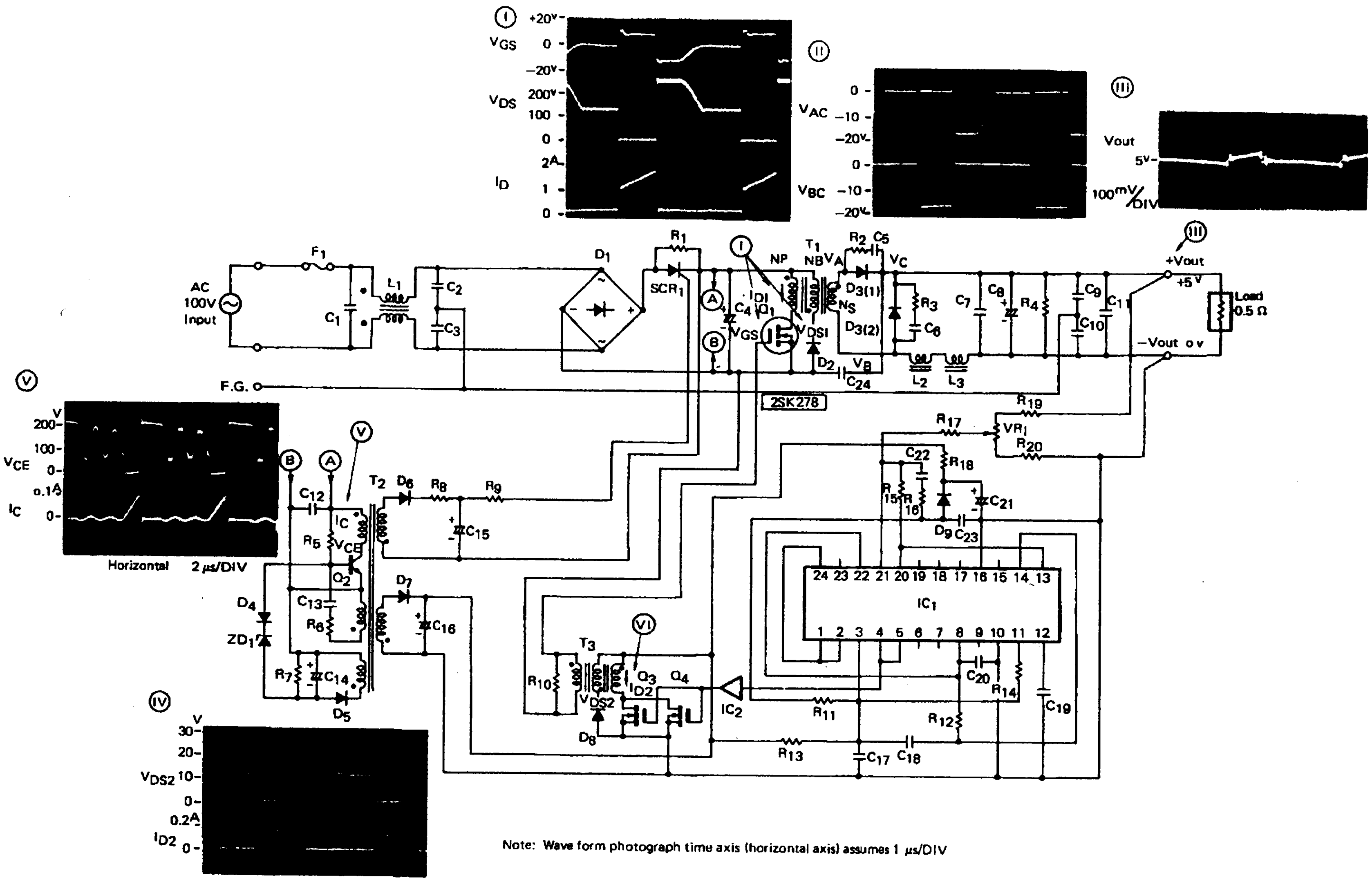
Conditions
Vin=100 V (AC 50 Hz)
Vout=5 V at Iout=10 A

Fig.10a Input/Output Characteristics and Efficiency vs. Output Current Conditions



Vin=80~120 V (AC 50 Hz)
Vout=5 V at Iout=10 A

Fig.10b Output Voltage and Efficiency vs. Input Voltage



Note: Wave form photograph time axis (horizontal axis) assumes 1 μs/DIV

Fig.11 Operating Waveforms of Trial Mode 1 Switching Regulator

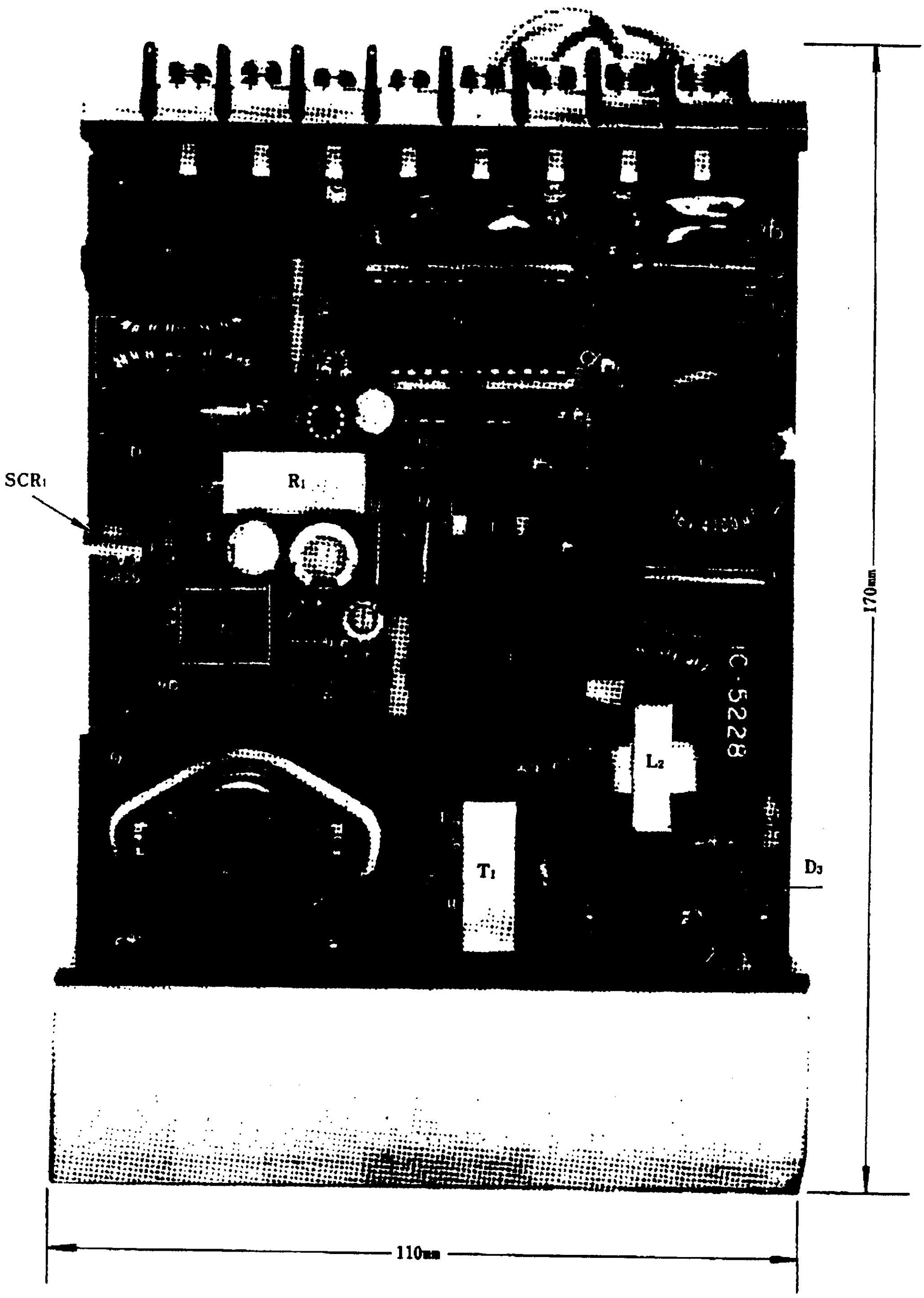


Fig. 12 Trial Model Switching Regulator External Appearance

5. SUMMARY

(1) Combined choke coil and its effect

In order to realize a faster response time making the most of the elevated operating frequency this switching regulator uses a pair of choke coils combined in such a way that, while one of them is saturated at prescribed amperage, the other of smaller L value remains unsaturated.

Fig. 14 shows an example of the advantage offered by such choke coil configuration at light load operation. Under this operating condition chole coil L_2 is not saturated. This causes I_D of invertor transistor Q_1 to incline less steeply, which in turn results in a reduced ripple current. The rewarding features of the combined choke coil are listed in Table 6.

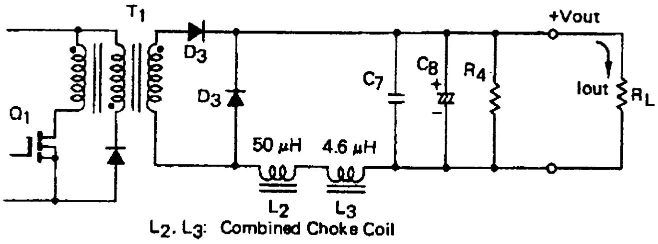


Fig.13a Secondary Side Rectifying Smoothing Circuit

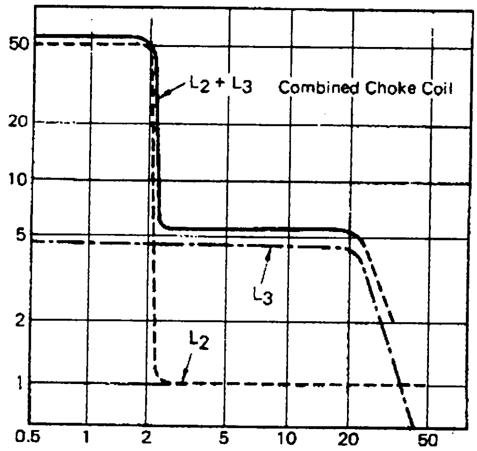


Fig.13b Combined Choke Coil Inductance Curves

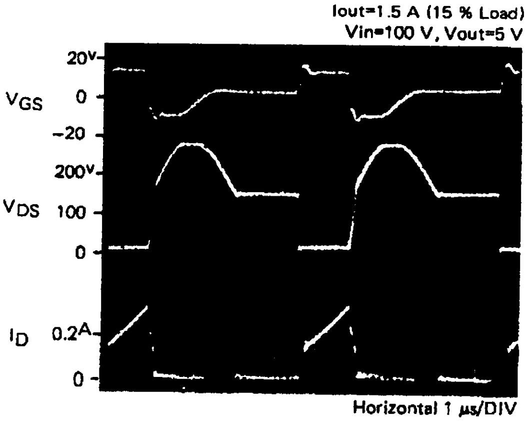
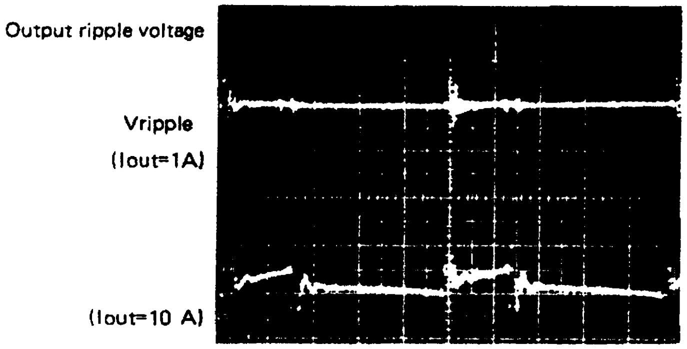


Fig.14 200 kHz Switching Regulator Operating Waveforms Under Light Load

Table 6. Rewarding Features of Combined Choke Coil

ITEM	CONTENTS
Reduced transient response time	As L_2 is saturated in the middle of operation, a faster output voltage transient response time is realized at load fluctuation than the case where a choke coil of same L value (50 μH) remains unsaturated.
Improved load regulation	Critical point moves farther toward the lighter end of load than the case where the saturating L_2 choke coil is absent. This improves load regulation almost to the same level as attained using a chole coil which has same L value as L_2 but does not saturate.
Improved stability	As critical point moves farther toward the lighter end of load than the case where L_2 is absent, the output ripple voltage does not rise in the load sweep test. This results in improved stability.
Reduced output ripple voltage under light load	The output ripple voltage is less pronounced than the case where L_2 is absent.
Improved efficiency under light load	L_2 works to reduce the ripple current of invertor transistor Q_1 under light load. This results in improved efficiency.

TABLE 6. REWARDING FEATURES OF COMBINED CHOKE COIL



Vertical Axis: 100 mV/DIV
Horizontal Axis: 1 µs/DIV

Fig. 15 Shows the Ripple Voltage Differences, Depending on the Amount of Output Current

– Transient Response Characteristics –

The transient response characteristics of output voltage when switching from light load to heavy load are discussed in the following pages.

Output Response

Suppose the switching regulator is put in operation as shown in Fig. 16 and load Rc is turned from OFF to ON by switching. Consider next how each part will behave.

As seen in Fig. 16-b, choke coil current I_L rises gradually after the switch is turned on. I_{D1} for $t = t_1$ is expressed as follows.

$$I_{D1} = \frac{V_S - V_{out} - V_F}{L} \cdot \tau_1 \quad \cdots\cdots\cdots\cdots\cdots \quad (1)$$

where V_S is the transformer secondary output voltage.

I_{D2} for $t = t_1 (= \tau_1 + \tau_2)$ is:

$$I_{D2} = I_1 = I_{D1} - \frac{V_{out} - V_F}{L} \cdot \tau_2 \quad \cdots\cdots\cdots\cdots \quad (2)$$

where V_F is the diode forward voltage.

Expressions (1) and (2) lead to:

$$I_1 = \frac{1}{L} \left\{ \tau 1 (V_S - V_{out} - V_F) - \tau 2 (V_{out} - V_F) \right\}$$

Assuming $\tau_1 = \tau_2 = \frac{T}{2}$,

$$I_1 = \frac{T}{2L} (V_S - 2V_{out}).$$

Therefore the value of I_L of choke coil in n-th cycle is:

$$I_{L(n)} = I_n = \frac{nT}{2L} (V_S \cdot 2V_{out}).$$

Conversely, taking $nT = t_S$ for the above expression,

$$t_S = \frac{2L \cdot In}{V_S - 2V_{out}} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (3)$$

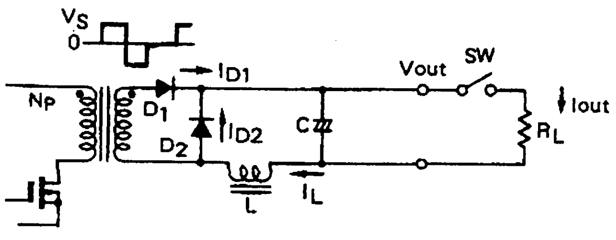
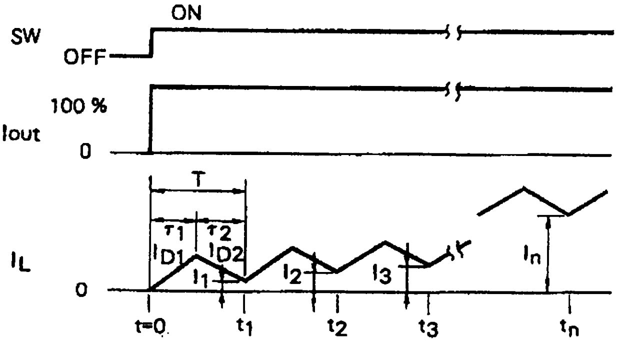


Fig.16a



τ_1: D_1 ON-State period (I_{D1} flowing in)
τ_2: D_2 ON-State period (I_{D2} flowing in)
T : cycle Rate

Fig.16b Step Response Waveform

The output voltage transient response to In in the circuit shown in the figure above is found next as shown in Fig. 17.

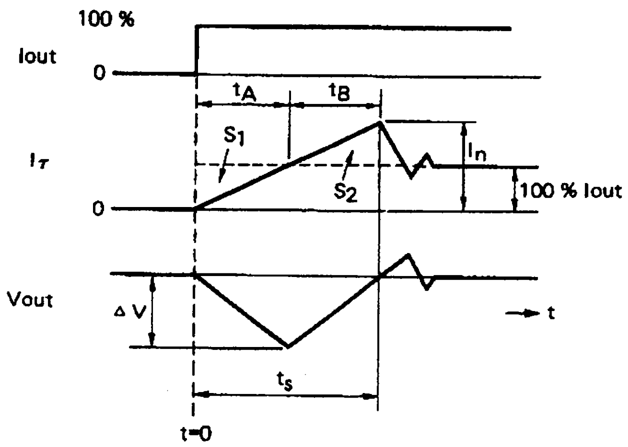


Fig.17 Output Voltage Transient Response Diagram

In rises linearly for t = 0 but an electric charge corresponding to area S_1 must be added in order to supply a certain amount of current (Iout) to the load. The electric charge corresponding to S_1 is to be obtained in the form of a discharge from capacitor C. This means, however, that the voltage across capacitor C suffers voltage drop ΔV corresponding to the discharge.

S_1, the amount of electric charge to be added to make up for linear but gradual increase of In, is expressed:

$$S_1 = \frac{1}{2} I_{out} \cdot t_A \text{ while } S_1 = S_2,\ t_A = t_B = \frac{t_S}{2} \text{ and } I_n = 2I_{out}.$$

As voltage drop ΔV across capacitor C corresponds to the amount of discharge from the capacitor, which in turn equals S_1,

$Q_C = C\Delta V = S_1$ where Q_C is the discharge from capacitor C.

$$\text{Therefore } \Delta V = \frac{I_{out} \cdot t_A}{2C} = \frac{I_{out} \cdot t_S}{4C} \quad \cdots\cdots\cdots\cdots \quad (4)$$

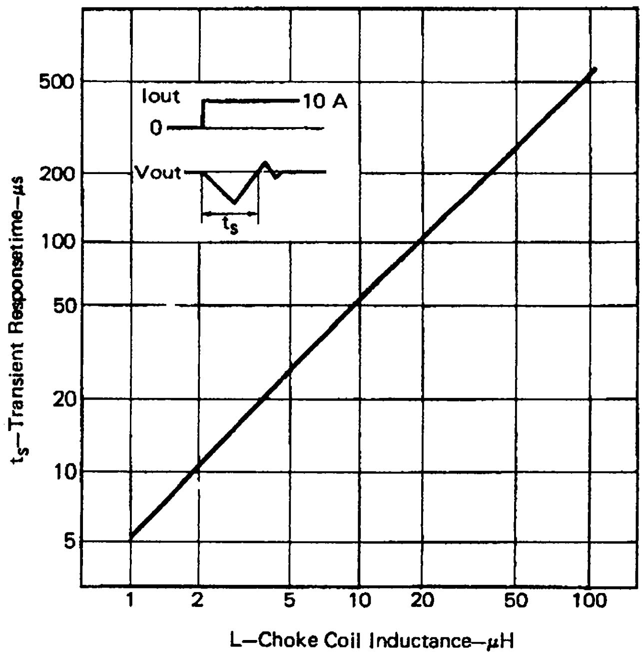
Putting Expression (3) in Expression (4),

$$\Delta V = -\frac{L \cdot I_{out}^2}{2C\,(V_S - 2V_{out})} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (5)$$

Rewriting Expression (3),

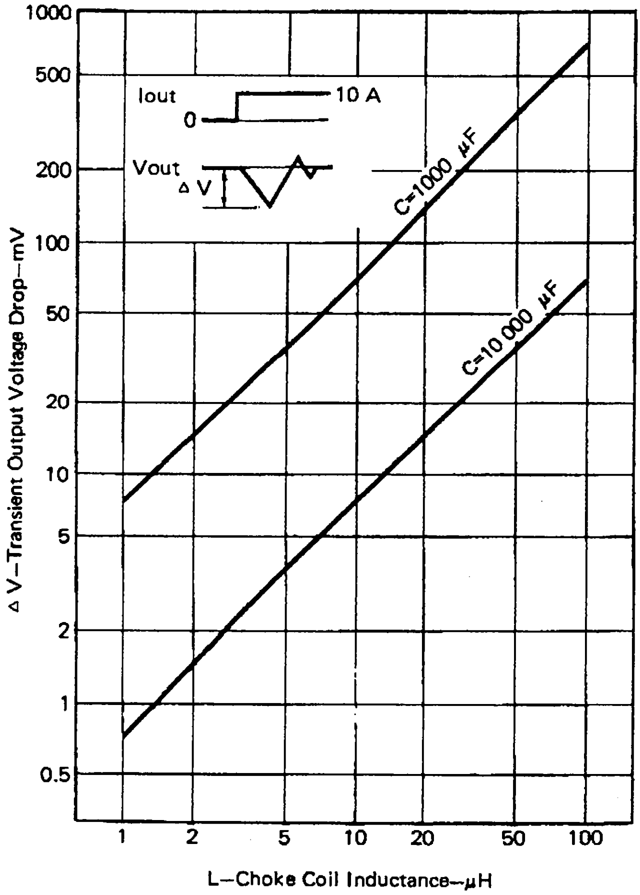
$$t_S = \frac{4L \cdot I_{out}}{V_S - 2V_{out}} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (6)$$

Therefore the relationship between transient response time constant t_S and choke coil inductance L and its counterpart between output voltage drop ΔV and choke coil inductance L are found as shown in Figs. 18-a and -b, using expressions (5) and (6).



Conditions
Vin=100 V
Vs=17 V, Vout=5 V
Iout=10 A

Fig.18a L vs. ts Characteristics



Conditions
Vin=100 V
Vs=17 V, Vout=5 V
Iout=10 A

Fig.18b L vs. ΔV Characteristics

Actual ΔV is subjected to the influence of line impedance up to the output terminal due to the presence of the smoothing capacitor as shown in the circuit of Fig. 19-a, and acts on the response waveform as shown in Fig. 19-b.

In order to abate this influence, it is necessary to reduce $r\ell$ as much as possible (less than 2–3 mΩ for 10 A application).

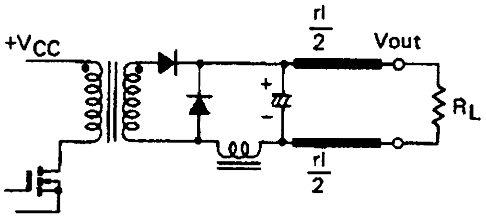


Fig.19a Circuit

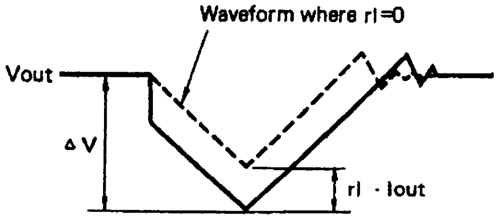


Fig.19b Response Waveform

Actual Example of Transient Response Characteristics

The output circuit configuration of this switching regulator is shown in Fig. 20. Response waveforms recorded for the load step from 0 to 100 % are shown in Fig. 21.

As seen in Fig. 21, this switching regulator realizes output response time $t_S \fallingdotseq 50\ \mu s$, which is much faster than that of previous switching regulators having the operating frequency of 20 kHz or so.

The output circuit of this switching regulator contains a combined choke coil which consists of choke coils L_2 and L_3. Choke coil L_3 has a relatively large L value of 50 μH but is saturated at 2 A or thereabout. As a result, its influence on the transient response characteristics is extremely reduced.

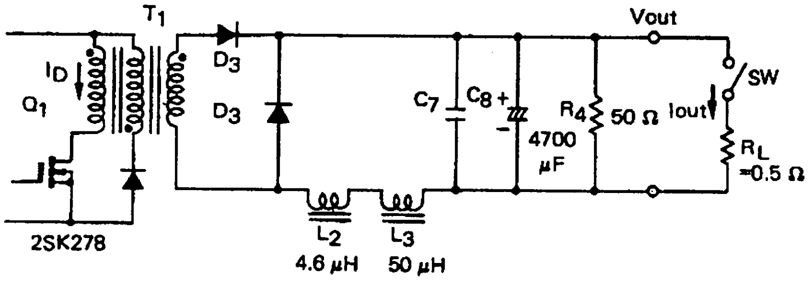
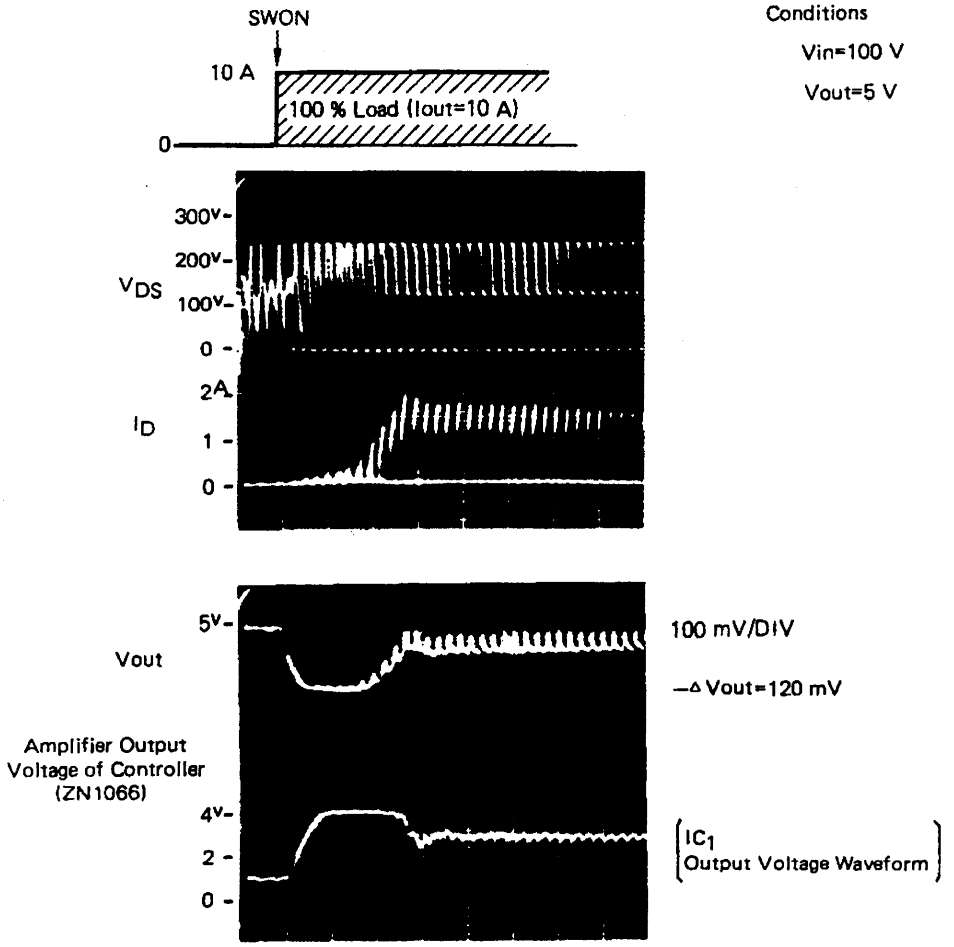


Fig.20 Forward Type Switching Regulator Circuit Configulation



Conditions
Vin=100 V
Vout=5 V

Fig.21 Output Voltage Transient Response Characteristics for 0 to 100 % Load Step Test

Please note our new name,
NEC Corporation
starting April 1, 1983.

Nippon Electric Co.,Ltd.

NEC Building, 33-1, Shiba Gochome, Minato-ku, Tokyo 108, Japan
Tel.: Tokyo 454—1111
Telex Address: NECTOK J22686
Cable Address: MICROPHONE TOKYO

TLA
MAR. - 20
Printed in J